KWIK CIRCUIT FAQ

ADC Analog Front End (AFE) for RTD Sensors

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FAQ: ADC Analog Front End (AFE) for RTD Sensors

Introduction

This *KWIK* (*K*now-how *W*ith *I*ntegrated *K*nowledge) Circuit application note provides a step-by-step guide to addressing a specific design challenge. For a given set of application circuit requirements, it illustrates how these are addressed using generic formulae and makes them easily scalable to other similar application specifications.

A practice often used in industry is to use a common ADC for a variety of sensors required in a particular application, and then develop a unique Analog Front End (AFE) for each of those sensors. This article will focus on the AFE for a 3-wire RTD which can be used with several RTD material types.

Design Specifications

The key design specifications are shown in Table 1. An ADC resolution of 16-bits, using a 2.5v reference, will permit a temperature resolution of 0.5 °F for the 10-ohm copper RTD and finer resolution for the other RTD types. Figure 1 is a block diagram of the circuit with the AFE contained within the dashed lines. A 1mA excitation current is a typical value used in an RTD design, as it nearly fills the ADC input range, when the RTD is at its maximum value, and at the same time minimizes the self-heating error in the RTD. Figure 2 is a detailed schematic of the AFE.

The term RTD stands for Resistance Temperature Device and is typically a wire-wound device with a moderate, positive, temperature coefficient of resistance. Various metals are used for the wire with platinum being the most widely used because of its high stability and large temperature range. Other metals used in RTD's are nickel and copper. For a given RTD type the average slope of resistance versus temperature between 0°C and 100°C is referred to as alpha. For the platinum RTD there is no single standard for alpha and values of 0.003923, 0.003850, and 0.00392 can be found. RTD's are available in 2, 3, and 4-wire configurations. The "lead" wires going to the RTD have resistance which cannot be ignored, since the RTD is a resistive device, any extraneous resistance in its circuit will cause an error in its temperature indication. Most RTD signal conditioning circuits provide a method to compensate for the lead wire resistance. If a circuit does compensate for lead wire resistance, then a possible source of error is the mismatch between each of the wires between the RTD and the signal conditioner. For the 100-ohm platinum RTD a mismatch of 0.38 ohms will results in an error of 1°C. For the 10-ohm copper RTD it would require a mismatch of only 0.04 ohms to cause the same error.

Table 1. Design Specifications

Input Range	Accuracy	Resolution	Excitation Current	Supplies Vdd/Vee	Vref
1-650 ohms	0.025% of FS	10mΩ/bit @ 16 bits unipolar 100Ω Pt 0.06°F (0.03°C) 120Ω Ni 0.025°F (0.014°C) 10Ω Cu 0.45°F (0.25°C)	1mA	±15V	+2.5V

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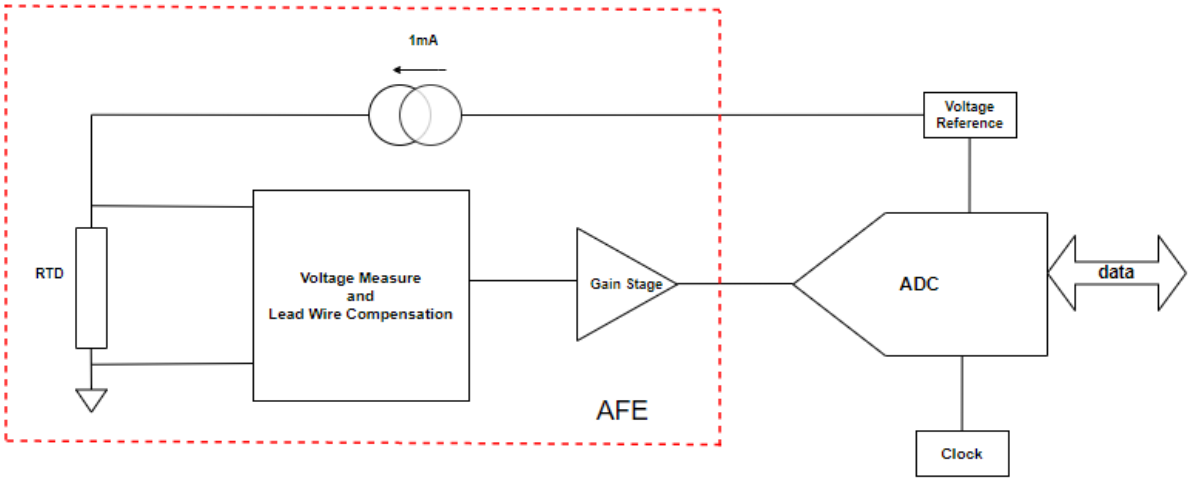

Figure 1. Block Diagram

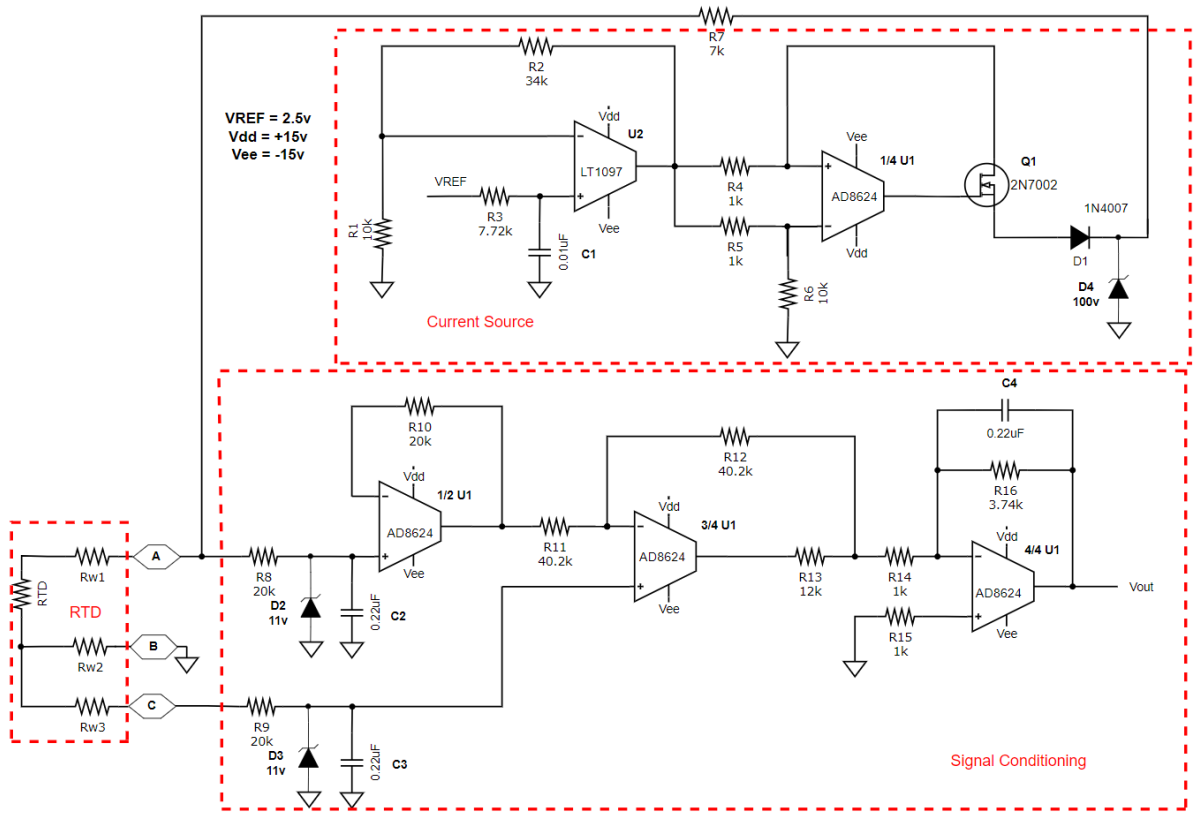

Figure 2. Detailed schematic of the AFE

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Design Description

This design translates the resistance of the RTD into a voltage by passing a constant, known current, through the sensor and measuring the resultant voltage drop. This design makes use of several precision elements to achieve the desired accuracy and to minimize the output voltage drift over a -40°C to 85°C operating temperature range. The elements comprising the design include a precision quad op-amp, a precision single op-amp, a custom resistor network, which provides resistor pairs that exhibit a very low matching temperature coefficient (tempco) of resistance of 5ppm/°C and a resistor ratio of 0.5%. The design performs lead wire compensation and provides an indication of an open sensor.

Design Tips / Considerations

1. Several resistor manufacturers offer a matched pair of resistors in a variety of packages. Some of these manufactures only offer a small set of values to choose from, while others allow a choice of any values you require, as long as the values are within a certain range. An example product would be the CNN series from Koa Speer, which allows for any two resistors between 1k and 100k with a relative TCR of 5ppm/°C and a resistance ratio of 0.05% or 0.1%. This type of product would lend itself to R1/R2, R4/R5, R11/R12, and R14/R16.
2. R7 should be a high wattage resistor, perhaps 3 watts, if input overvoltage protection to 120vac is desired.
3. R8 and R9 should be high wattage resistors, perhaps 2 watts, if input overvoltage protection to 120vac is desired.
4. R6 should be a discrete 5ppm/°C, 0.5% absolute accuracy (or better), 1/8 watt resistor.
5. R3, R10, and R15 can be 1% resistors.
6. For a 16-bit ADC with a 2.5v reference the LSB for a unipolar input has a weight of 38uV.

Design Procedure

(refer to Figure 2)

1. RTD 1mA Excitation Current

An RTD excitation current of 1mA was chosen as a balance between minimizing errors due to self-heating effects of the RTD element and between the resolution desired. A 100-ohm platinum RTD at 700°C will have a resistance of 345 ohms. A 1mA current will result in the dissipation of 0.345mW. For a platinum sensor that exhibits 0.34°C of error per milliwatt of power dissipation this results in a self-heating error of about 0.117°C or 4 LSB's. The 1mA current source as designed has a compliance voltage of about 9v as shown in the following equation,

$$\text{Compliance voltage} = 11v - V_{R4} - Vds(Q1) - V_{d1} \approx 9v \quad \text{(eq. 1)}$$

This information is used to determine the value of R7 (7k) which is used to limit the current that would be drawn from or sourced into the RTD circuit should 120vac inadvertently be applied to the field terminals. The generation of the excitation current begins with a 2.5v reference voltage which is gained up to 11vdc by U2. The output of U2 is applied across a voltage divider comprised of a 1k and a 10k resistor which results in a 1mA current flowing through the divider. The voltage developed across the 10k resistor in the divider acts as an input to the inverting terminal of ¼ U1. The amplifier, through its feedback network, forces its non-inverting input to be equal in potential to its inverting input which is 10vdc. Within the feedback network is an n-channel MOSFET (Q1) which, together with ¼ U1 form a voltage-to-current converter and Q1 provides the required 180° of phase shift necessary to stabilize the op-amp. As the op-amp turns on Q1, a current then flows through R4, the channel of Q1, D1, R7, the RTD, and then to ground. The current is supplied by op-amp U1 and is set by the voltage drop across R5 at 1mA (i.e., 1 volt across a 1k). This constant current source will work properly if the sum of all voltage drops along the current path does not attempt to exceed the 9v compliance voltage of the current source. The resistor R7 is for input protection of the circuit on that leg. After accounting for the 7v drop across R7 the limit on the maximum RTD resistance (including lead wire resistance) that this circuit will support is approximately 1668 ohms. Other sections of the design will limit the RTD resistance (excluding lead-wire resistance) to about 660 ohms so the design can accommodate up to 500-ohms/leg of lead wire resistance.

2. RTD Voltage Measure and Lead Wire Compensation

The voltage developed across the RTD is buffered by ½ U1 then applied to the inverting input of ¾ U1. Port B is normally connected to port C through two lengths of the RTD lead-wires. The RTD excitation current flows out port A, through the RTD, and returns through port B. Ideally no current will flow in the lead-wire connected to port C Because it is connected to the non-inverting input of ¾ U1which has a very large input impedance. Therefore, the voltage present at the non-inverting input of ¾ U1 will represent the voltage drop due to the resistance of the lead-wire connected to port B. The voltage at the output of ½ U1 represents the sum of the voltage across the lead-wire connected to

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port A, the RTD, and across the lead-wire connected to port B. The voltage on the right-hand side of R13 (12k) is given by,

$$V = 2*V_{Rw2} – (V_{Rw1} + V_{rtd} + V_{Rw2}) = -V_{rtd} \text{ (Eq. 2)}$$

As can be seen by equation 2 the voltage drop across the lead-wires has been removed, this is referred to as lead-wire compensation. The accuracy of the lead-wire compensation depends on how well matched the cables connected to port A and port B are and 3-wire cables are commercially available, specifically for extending the length of an RTD.

3. *Final Gain Stage*

The final stage of the design provides a nominal gain of -3.74 which is selected to meet the input range of the ADC which is assumed to be 0-2.5v and supports resistances between 0-668 ohms as shown below,

max ADC input voltage/gain of final stage = max measurable voltage across RTD

2.5/3.74 = 0.668449v

Then

max measurable voltage across RTD * RTD current = max RTD resistance

0.668449 * 1mA = 668.449 ohms (Eq. 3)

4. *Input Protection*

If the application for a RTD is in the industrial market (refinery, automotive, food processing, etc.) some level of input protection should be considered. A few components have been shown in this design to provide protection of this circuit from an overvoltage condition at any of the input/field terminals identified as ports A-C. The 1mA current source is protected against positive over voltages at port A by diode D1. If the positive overvoltage exceeds a certain value (100v has been assumed here) then the Zener diode D4 begins to conduct. Zener diode D4 also protects during a negative over voltage condition. In all cases described so far resistor R7 (7k) will limit the current. Zener diodes D2 and D3 protect the voltage measurement circuit against over and under voltage conditions on ports A and C. Both Zener diodes show a 20k resistor for current limiting (R8 and R9). The level of heat sinking afforded these protective components will determine the actual level of protection they can provide.

A different over voltage condition that the module needs protection against is the case where this circuit is powered up, but the RTD has not been connected as yet. In that scenario the current source will be attempting to force 1mA of current into an open circuit and as a result it will drive the voltage at port A as positive as it can which could be close to 11v. This voltage would then be gained up and appear at Vout as a voltage near 14.5v then be applied to the ADC input. ADC inputs are protected against over voltages by ESD diodes which would turn on and sink current from 4/4 U1 as a result. A simple method to protect against this scenario and minimize the amount of current that the ESD diodes in the ADC will see is described next. This overvoltage protection is accomplished by placing R13 (12k) in the feedback loop of ¾ U1 as shown. As the overvoltage event is occurring excess current will be drawn through R13 which will reduce the voltage seen at the input of the gain stage 4/4 U1.

Design Simulations

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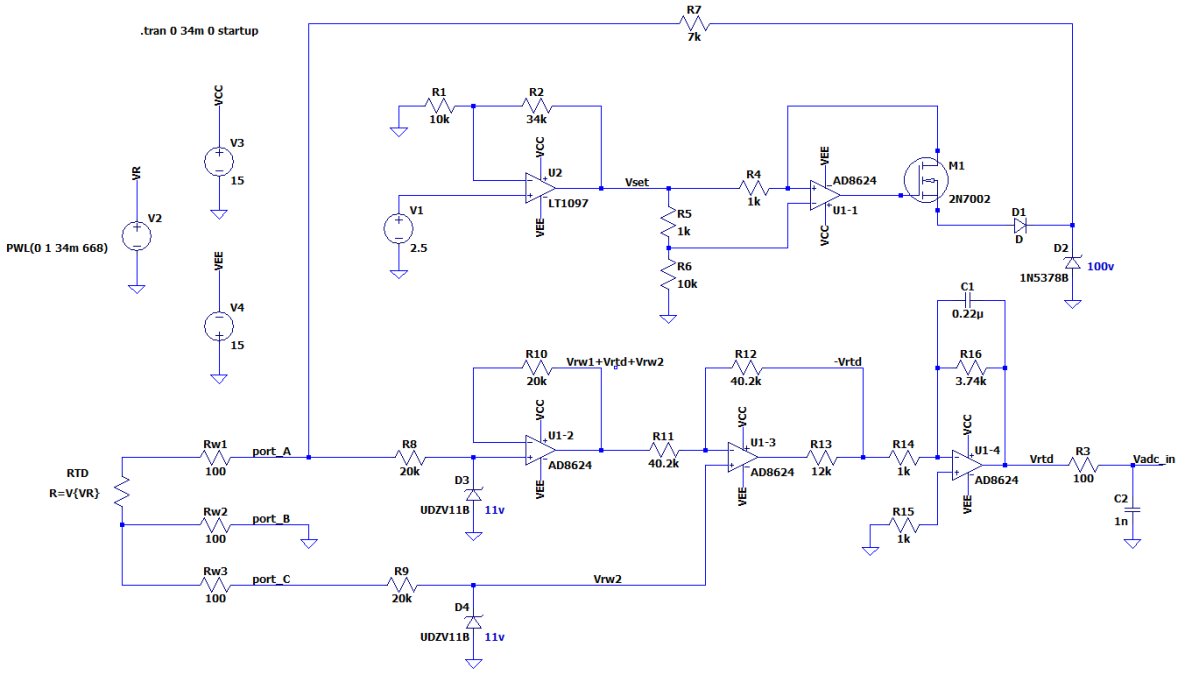

Figure 3. LTspice simulation schematic of the AFE

The simulation in Figure 4 shows that the voltage drop due to the lead wire (across Rw2) is 100mV (green trace) and that the voltage at the node labeled Vrw1 + Vrtd + Vrw2 (blue trace) goes from about 200mV, when the RTD is 1 ohm to 868mV, when the RTD is 668 ohms. In this time domain simulation, the value of the RTD is defined to be a variable whose value is swept by specifying a swept node voltage for the resistance of that RTD. In the schematic you will see that the RTD has a value of V{VR} and you will also see that VR is a net name for the output of voltage source V2. This voltage source is defined to be a piece-wise linear (PWL) source whose value is 1V at time 0 and 668V at time 34ms. The simulation is then run for 34ms.

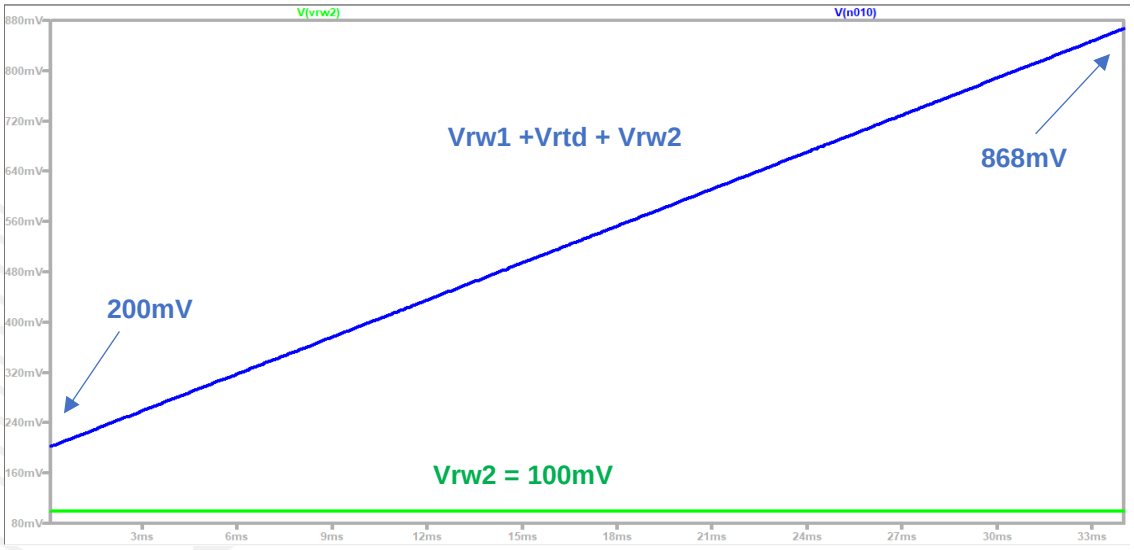

Figure 4. Simulation result showing the inputs of U1-3

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The simulation in Figure 5 shows the voltage at the output of the summer U1-3 at node -Vrtd (green trace) and after a gain of -3.74 is applied to that signal (red trace) to fill the 0-2.5v ADC input range.

In the simulation of Figure 6, the RTD is not connected and R13 is made very small to demonstrate what will happen on power-up. This allows you to see that the voltage at the node “Vadc in” (red trace in figure 7) will go to the upper rail of U1-4 which is about 14.56v. Some form of protection is needed to prevent this from happening and one proposed method is illustrated by restoring R13 to it’s 12k value, as shown in Figure 8. With R13 resized to be 12k and the simulation reran you can see the node “adc_in” only goes to 3.83v so if the ADC ESD diode is clamping to a +5v supply it will not be turned on during this event.

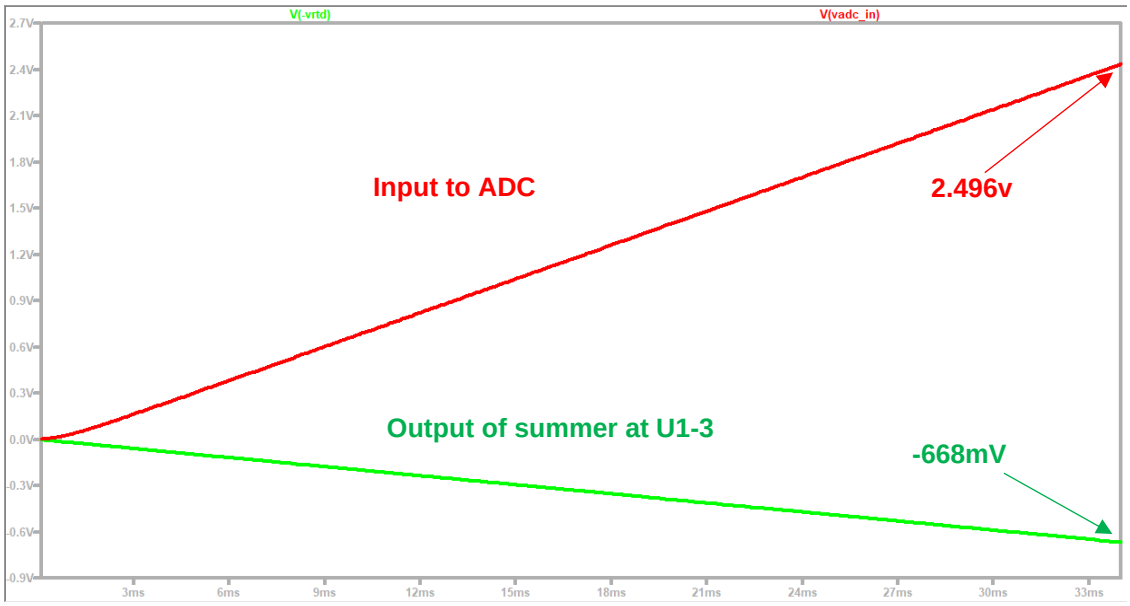

Figure 5. Simulation results showing the output of U1-3 and U1-4

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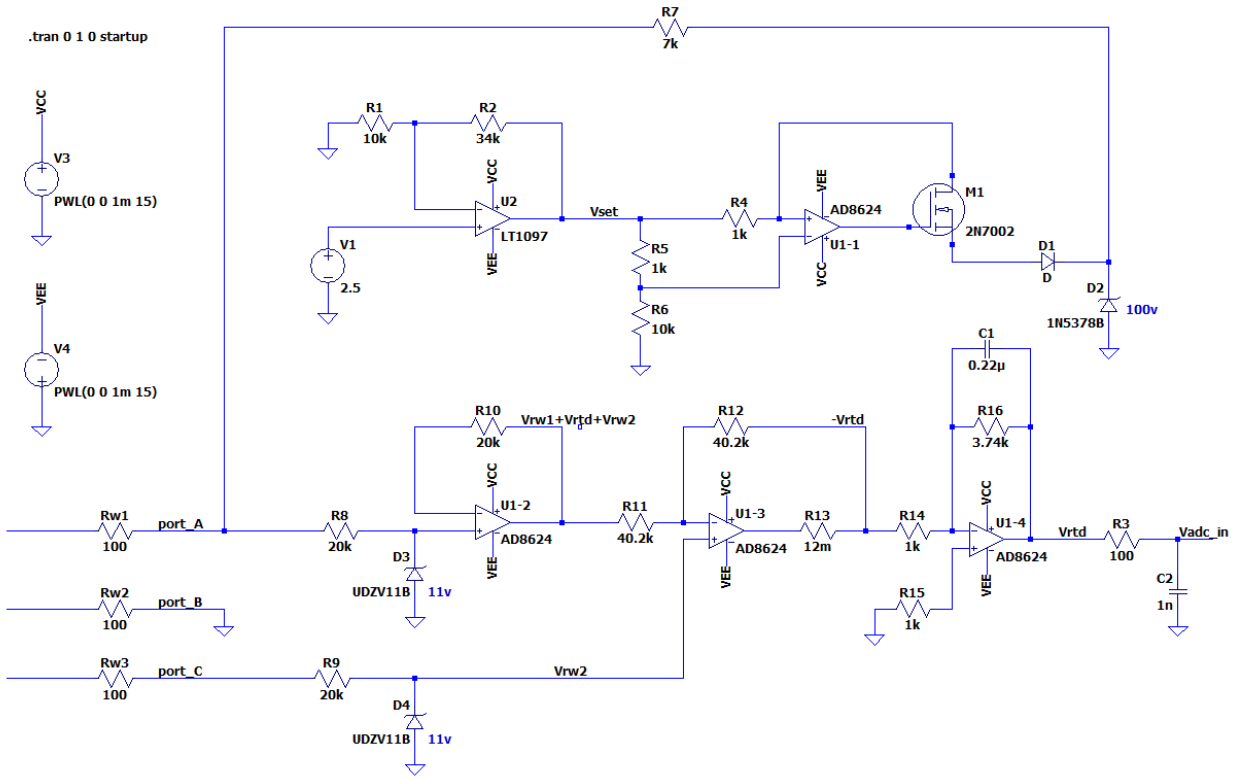

Figure 6. Simulation schematic for an open sensor

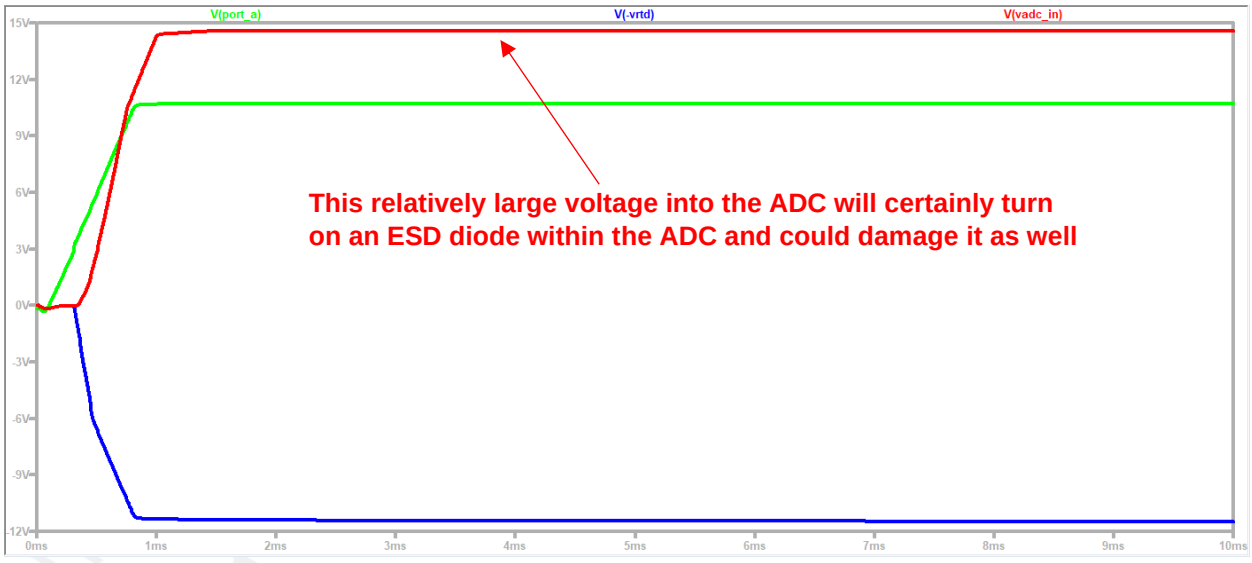

Figure 7. Power-up simulation without an RTD connected and R13 made very small (12 milliohms)

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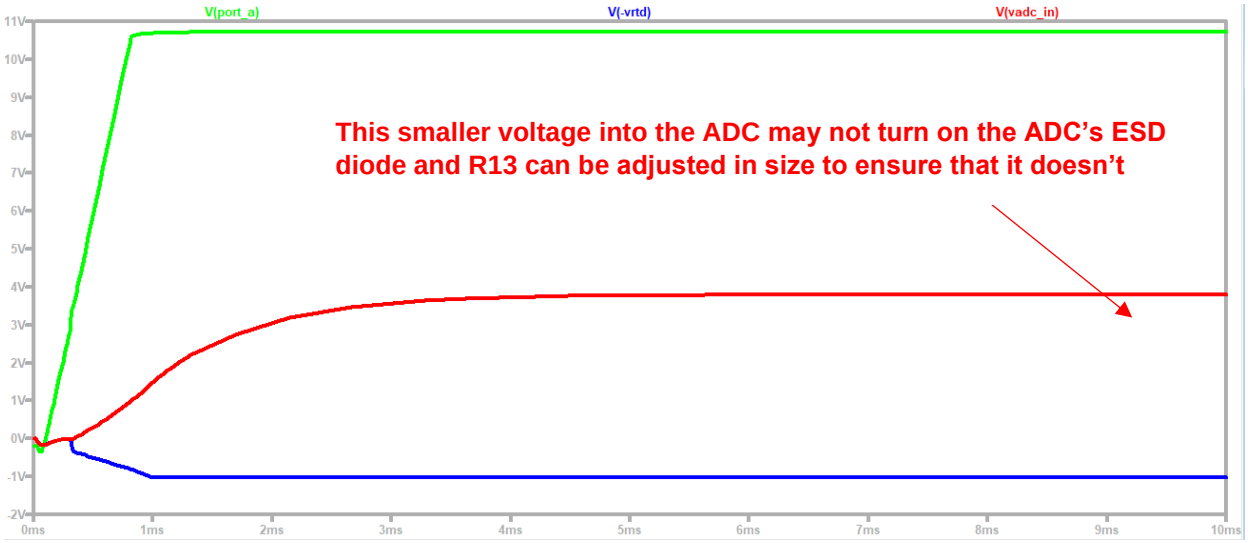

Figure 8. Power-up simulation without an RTD connected and R13 made larger (12k ohms)

A quick check of the stability of the amplifier driving the current loop (U1-1) was done with the modified simulation schematic shown Figure 9. The components (R100, R101, C100) were added to make the output impedance of U1-1 better match the output impedance plot found in the data sheet for the AD8624. The simulation result (Figure 10) shows adequate loop gain phase margin at ambient temperature.

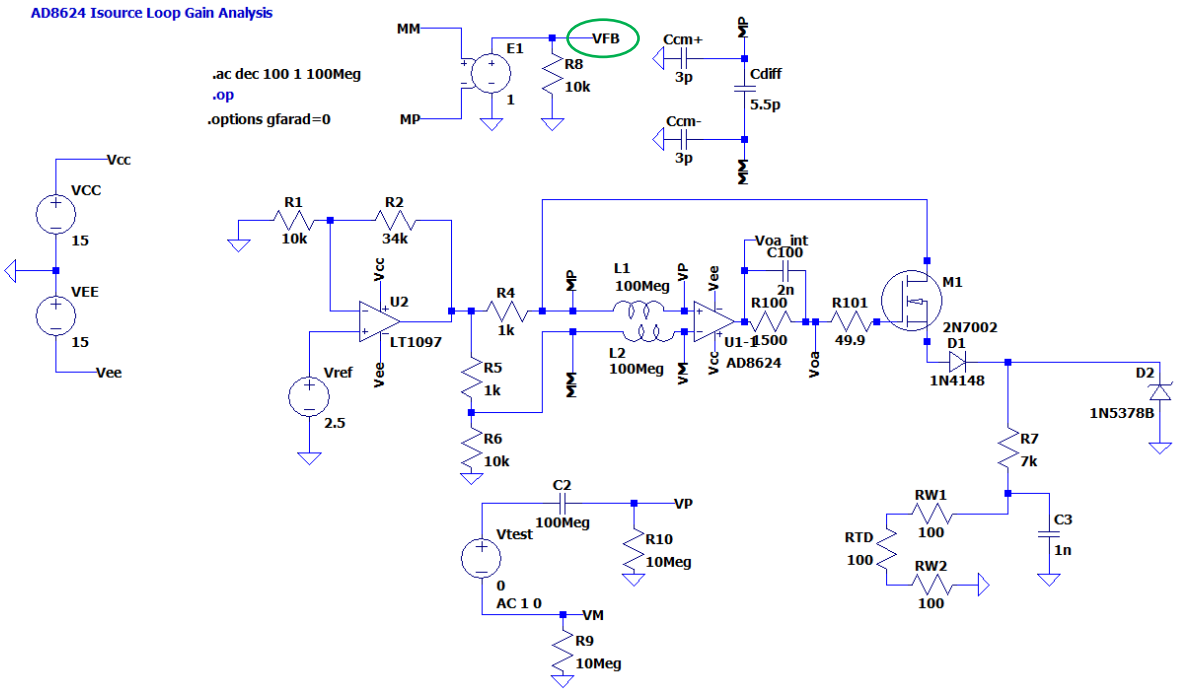

Figure 9 Simulation schematic for determining loop gain and phase margin

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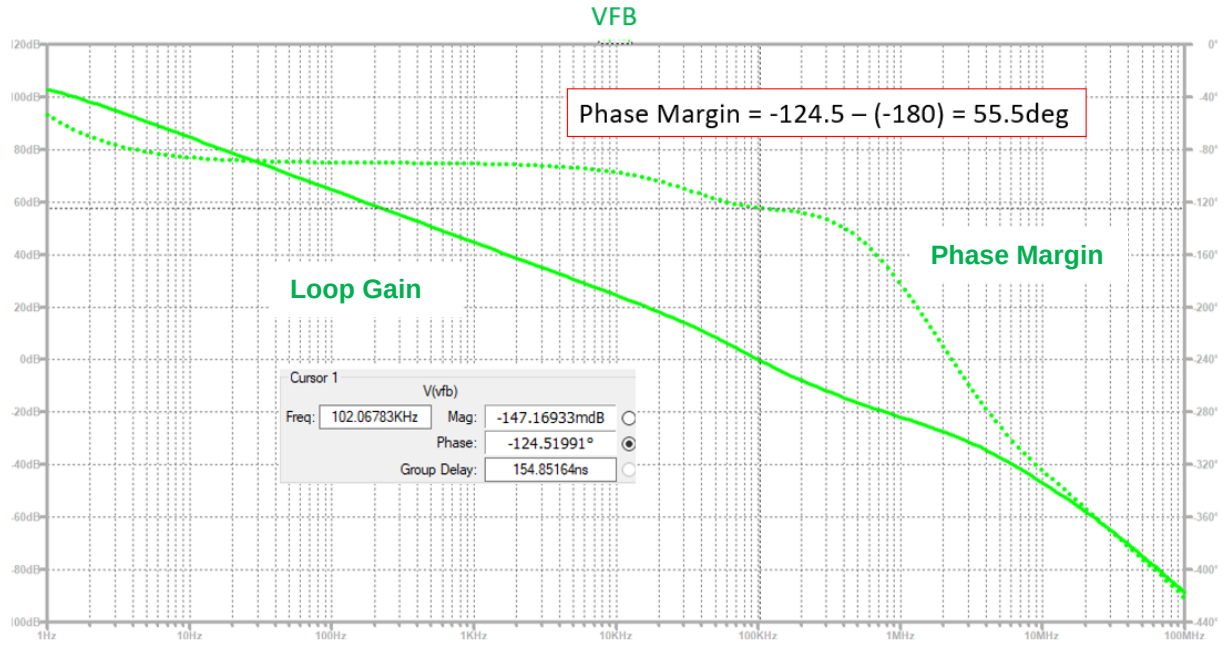

Figure 10 – Loop Gain and Phase Margin

Design Devices

Table 2.

Part Number	Vos	Input Bias Current Ib	Offset Voltage Drift TCVos	Input Offset Current Ios
AD8624	125uV max an 25C	200pA max at 25C	1.2uV/C max	200pA max at 25C
LT1097	50uV max an 25C	250pA max at 25C	1.0uV/C max	250pA max at 25C

References

RTD Interfacing and Linearization Using an ADuC8xx MicroConverter
https://www.analog.com/media/en/technical-documentation/application-notes/AN709_0.pdf

RTD Interfacing and Linearization Using an ADuC706x Microcontroller
https://www.analog.com/media/en/technical-documentation/application-notes/AN-0970.pdf

LTspice

LTspice® is a high-performance SPICE III simulator, schematic capture and waveform viewer with enhancements and models for easing the simulation of switching regulator, linear, and signal chain circuits. LTspice can be downloaded from the website www.analog.com.

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