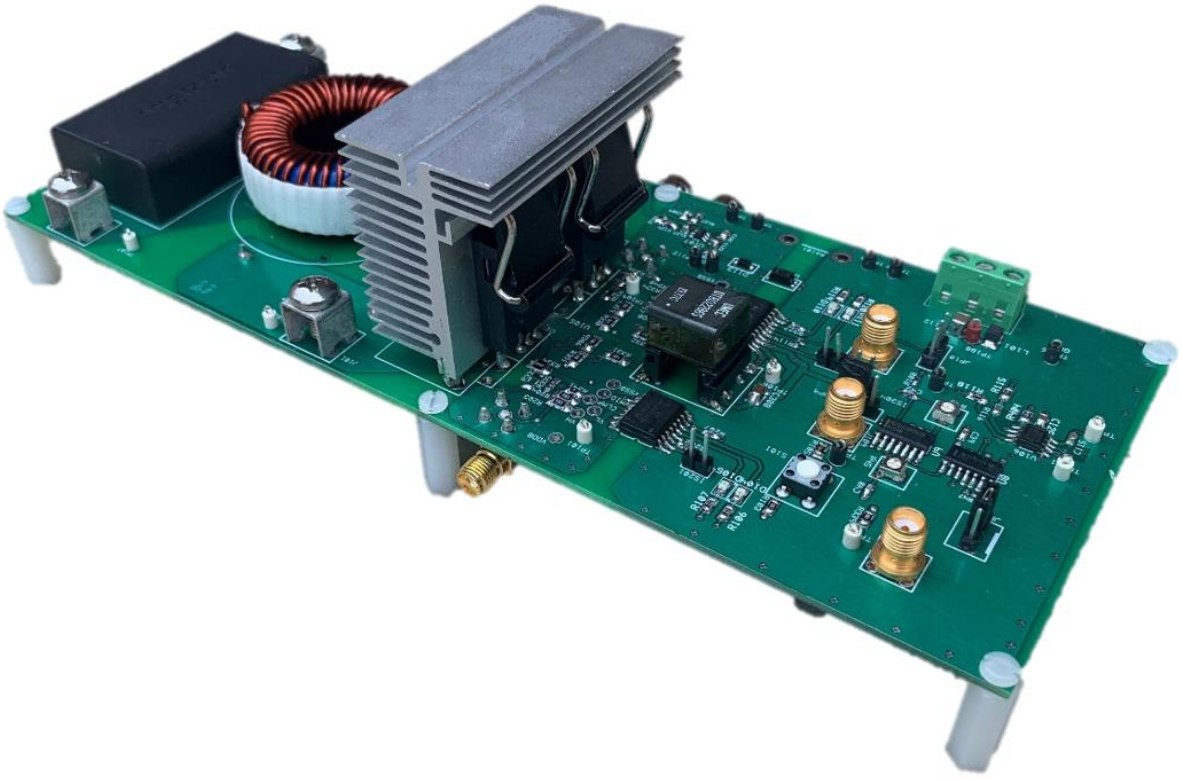
Test Report: Driving Cree® C3M™ SiC MOSFETs with Silicon Labs® Si828x Gate Drivers in applications requiring short-circuit protection



PRD-02344 Rev 1

1. Introduction

The main purpose of this test report prepared jointly by Cree (through its Wolfspeed business division) and Silicon Labs is to document the results of testing performed to characterize the short circuit behavior of Cree® C3M™ Silicon Carbide (SiC) MOSFETs when driven with Silicon Labs® Si828x gate drivers. It demonstrates the fast short-circuit detection of the driver IC coupled with the robustness of the SiC MOSFET design allowing the system to survive extreme short-circuit conditions.

While the short-circuit protection is the main subject of this report, the overall performance of the gate driver including common mode transient immunity (CMTI) and cross-talk (or Miller) immunity in a hard-switched synchronous boost application were evaluated as well.

This document may be used to assess the feasibility of new designs using Cree C3M SiC MOSFETs with Silicon Labs Si828x gate drivers in hard-switched applications requiring short-circuit protection. The specific Silicon Labs drivers evaluated in this test were Si8281 and Si8285 but all of their Si828x drivers offer the same short-circuit protection and CMTI capabilities.

2. Background

The numerous benefits of SiC MOSFETs have been well documented. However, one significant difference of SiC MOSFETS compared to Silicon IGBTs is that SiC MOSFETs have a lower short-circuit withstand time. While this poses a design challenge, it can be overcome with good layout and a gate driver equipped with a fast desaturation (DESAT) detection circuit and soft shutdown.

The Si828x isolated gate driver's high drive current is sufficient to allow the SiC MOSFETs to be driven as fast as 100V/ns in this test setup. The high CMTI supports signal integrity during these fast transitions while an internal Miller clamp prevents any parasitic Miller capacitance induced turn on.

3. Testing

A HALF-BRIDGE EVALUATION BOARD WAS USED TO COMPLETE ALL THE TESTING. TWO DIFFERENT SILICON LABS GATE DRIVER ICS WERE USED AS SHOWN IN

Table 1.

Part #	Description	Function
Si8285CC-IS	Isolated gate driver with short circuit protection	High Side Gate Driver
Si8281CC-IS	Isolated gate driver with short circuit protection and on-chip DCDC	Low Side Gate Driver

TABLE 1: SILICON LABS® GATE DRIVER ICS TESTED

Two different Cree SiC MOSFETs were tested as shown in Table 2.

Part #	Description
C3M00651000K	1000V 65mohm TO-247-4
C3M0016120K	1200V 16mohm TO-247-4

TABLE 2: CREE® SIC MOSFETS TESTED

The half-bridge evaluation board used for these tests was developed by Silicon Labs. The reference design can be found at:

www.silabs.com/isolation/wolfspeed-partner-designs.html#si828x-wssic-halfbridge-refdesign

Note: *Silicon Labs prepared various documents, which may include a User's Guide or an Application Note, that describe the proper operation and safe usage of the half-bridge board that was used for these tests. Please review any documents that describe the use of this board that are located at* www.silabs.com/isolation/wolfspeed-partner-designs.html#si828x-wssic-halfbridge-refdesign *for information and warning statements about the proper usage of this board. YOU MUST READ ALL OF THE DOCUMENTS THAT APPLY TO THE BOARD AND ARE DESCRIBED IN THIS PARAGRAPH BEFORE YOU OPERATE THE EVALUATION BOARD. DEATH OR SERIOUS INJURY, INCLUDING ELECTROCUTION, ELECTRICAL SHOCK, OR SEVERE BURNS, CAN OCCUR IF THE EVALUATION BOARD IS IMPROPERLY USED OR IF PROPER SAFETY PRECAUTIONS ARE NOT FOLLOWED.*

3.1 Short Circuit Testing

Short circuit testing was performed by creating a low-impedance connection across the upper SiC MOSFET in the phase leg. This simulates a short-circuit failure of a semiconductor, transformer, inductor, motor, or other load depending on the topology. Under this condition, when the lower SiC MOSFET is turned on, the current rapidly increases and is only limited by the bus voltage, SiC MOSFET R_{DSon}, and parasitic inductance. This condition must be detected quickly and the SiC MOSFET gate must be turned off quickly to prevent damage to the SiC MOSFET due to overcurrent. However, turning the gate off too quickly can result in high V_{DS} overshoot which can also be destructive. Balancing these conflicting needs is done with a "soft-shutdown" technique.

Some applications require robust protection against short-circuit conditions. This is often required in motor drive applications, and any other application where a short-circuit may exist in the load. The purpose of the short-circuit protection is to stop cascading failures and protect the power semiconductors, allowing the system to be more easily serviced and returned to normal operation.

Board Setup:

This test was performed by placing a shorting wire across either the upper or lower SiC MOSFET Drain and Source pins (each were tested, and the results matched), and by placing the opposite SiC MOSFET (DUT) directly across the DC bus. The enable signal for the DUT was set high, and the part was turned on until the Si828x detected the short-circuit condition and turned it off. This condition simulated a pre-existing short in the system.

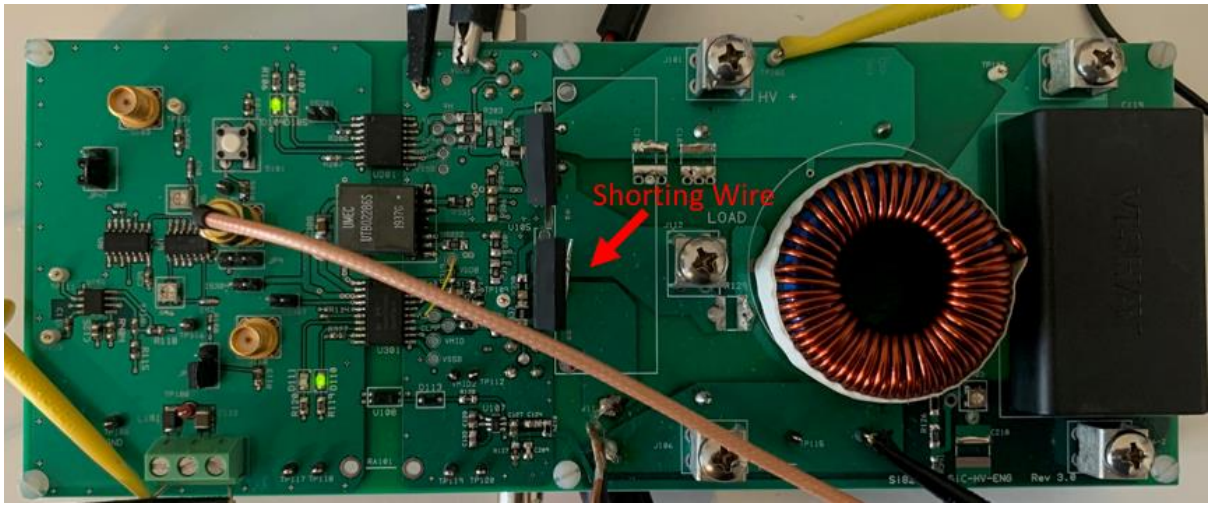


FIGURE 1: TEST SETUP WITH LOWER SIC MOSFET SHORTED (UPPER SIC MOSFET IS DUT)

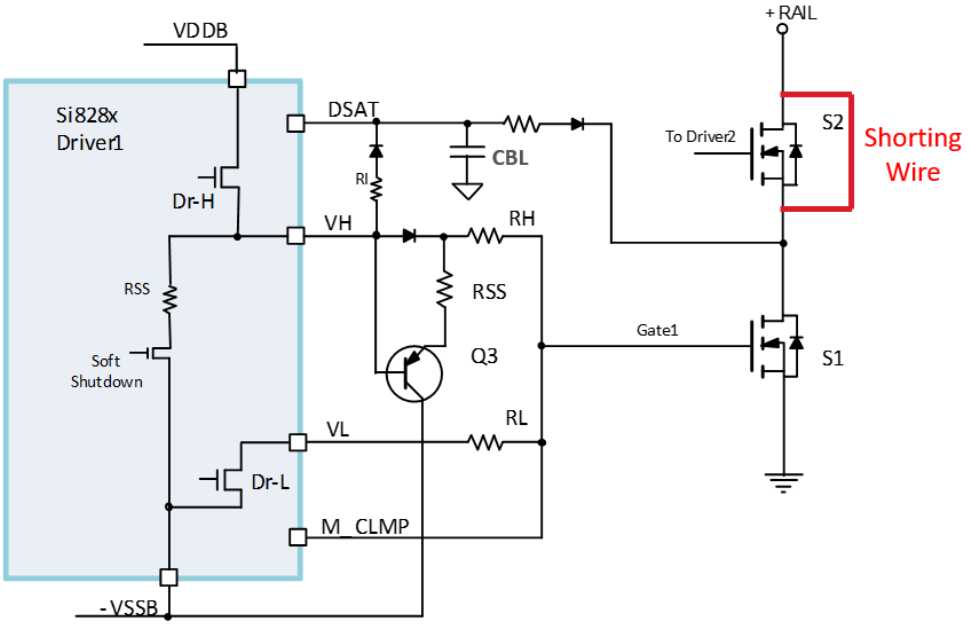


FIGURE 2: SIMPLIFIED DIAGRAM OF THE DRIVER CIRCUIT AND A SHORTED UPPER SIC MOSFET

Test Results:

Several different test conditions were used to demonstrate the flexibility of the DESAT protection on the Si828x. The soft-shutdown path on the Si828x has a built-in 50-ohm resistor. However, an external transistor (Q3) and soft-shutdown resistor (R_{SS}) can be added to accelerate the soft-shutdown turn off speed. The resistor RI can be used to accelerate the short circuit detection time without reducing the value of the desaturation capacitor, C_{BL}. C_{BL} is the blanking capacitor, which acts to filter out the turn-on transient of the SiC MOSFET during normal operation to prevent unexpected fault signal generation. Reducing C_{BL} too far reduces noise immunity and can create false fault trips. Silicon Labs Application Note 1288 details all the external enhancement circuits available to fine tune the circuit to the application.

The rate of rise of current in a short circuit condition will depend strongly on the impedance between the DC bus, the SiC MOSFET, and the short circuit. The testing described here placed the short circuit directly on the test board with minimal impedance, creating a very fast current rise. Similarly, the amount of voltage overshoot on turn-off depends strongly on the layout and impedance between the SiC MOSFET and the DC bus. In all test cases the driver safely turned off the SiC MOSFET before any damage occurred.

The first test used a Cree 65mOhm 1000V SiC MOSFET (P/N C3M00651000K) and the internal 50-ohm soft shut-down resistor. This configuration resulted in a fast, yet controlled shutdown of the SiC MOSFET. The total duration of the short-circuit current was approximately 530ns with a voltage overshoot of 150V on turn-off. For this SiC MOSFET, the Si828x internal 50-ohm soft-shutdown resistor is appropriate due to the relatively low gate charge, allowing for a well-controlled shutdown.

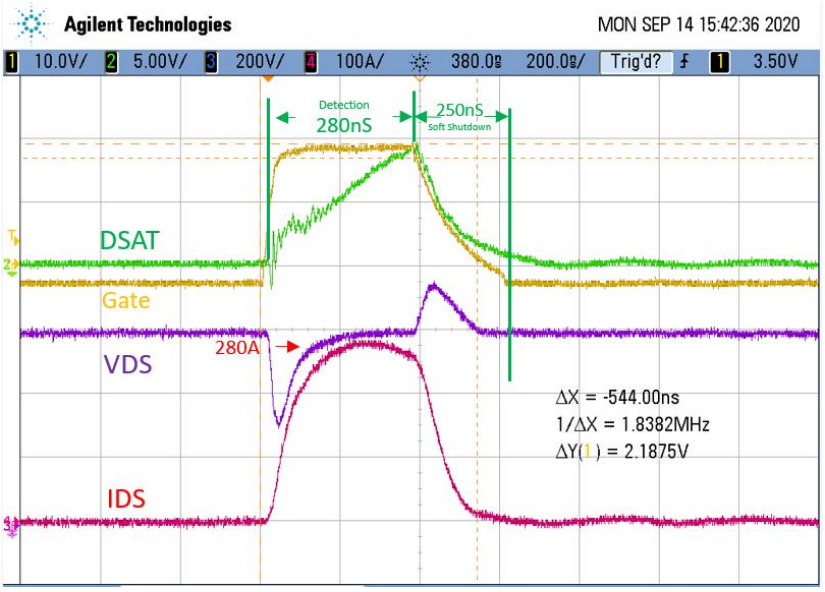


FIGURE 3: C3M0065100K WITH 50-OHM SOFT-SHUTDOWN

Next, the Cree 16mOhm 1200V SiC MOSFET (P/N C3M0016120K) was tested with two different external soft-shutdown resistors to demonstrate the tradeoffs when selecting R_{SS}. The first test used 30 ohms, and the second used 5 ohms. As you can see in Figure 4 below, the gate voltage came down much faster with a 5-ohm resistor as expected. While this caused the current to drop faster, the higher di/dt created a larger voltage overshoot on the SiC MOSFET drain. Selecting the appropriate R_{SS} for a given application is a balance between quickly terminating the short circuit condition and limiting the voltage overshoot to a safe level. Parasitic impedance in the system has a strong effect on this behavior.

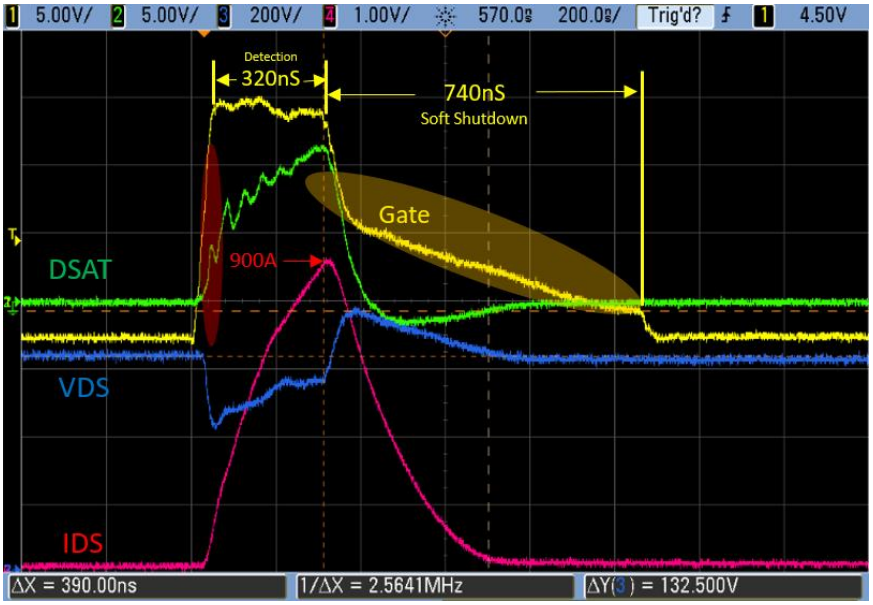


FIGURE 4: COMPARISON BETWEEN R_{SS}=30 OHMS (TOP) AND R_{SS}=5 OHMS (BOTTOM)

The final test was performed at a higher bus voltage which allowed the current to increase faster. Additionally, the C_{BL} capacitor was increased, lengthening the detection time. Under this condition, the driver was still able to shut the SiC MOSFET down before any damage occurred even though it took longer and reached a higher peak current.

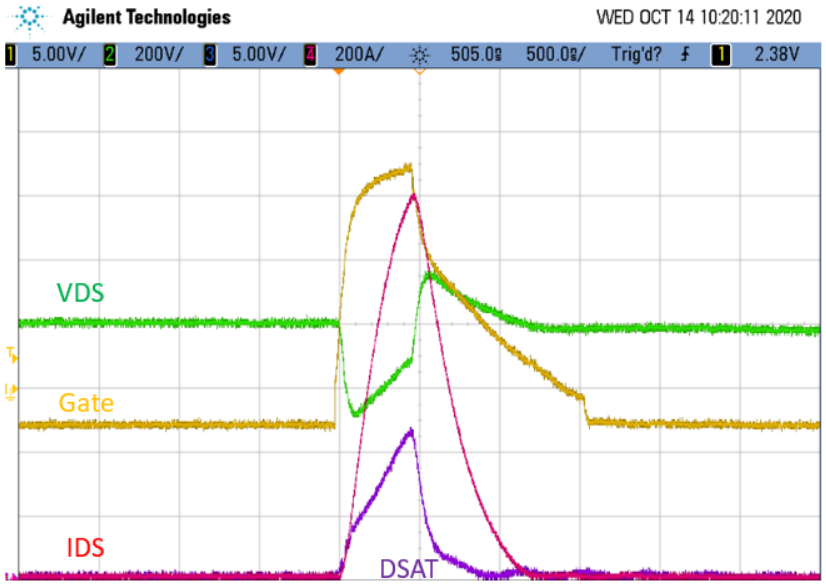


FIGURE 5: C3M0016120K SHORT CIRCUIT TEST WITH V_{BUS}=800V, R_{SS}=50, C_{BL}=390

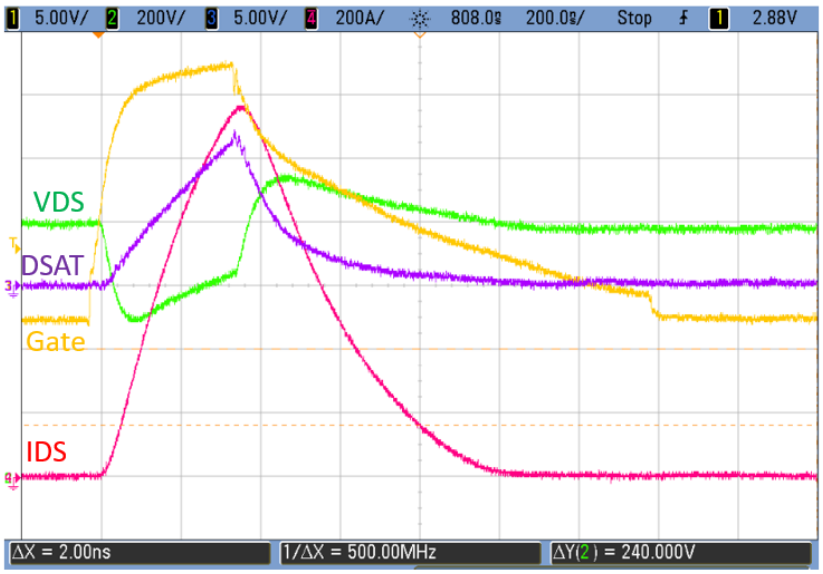


FIGURE 6: C3M0016120K SHORT CIRCUIT TEST WITH V_{BUS}=800V, R_{SS}=50, C_{BL}=270

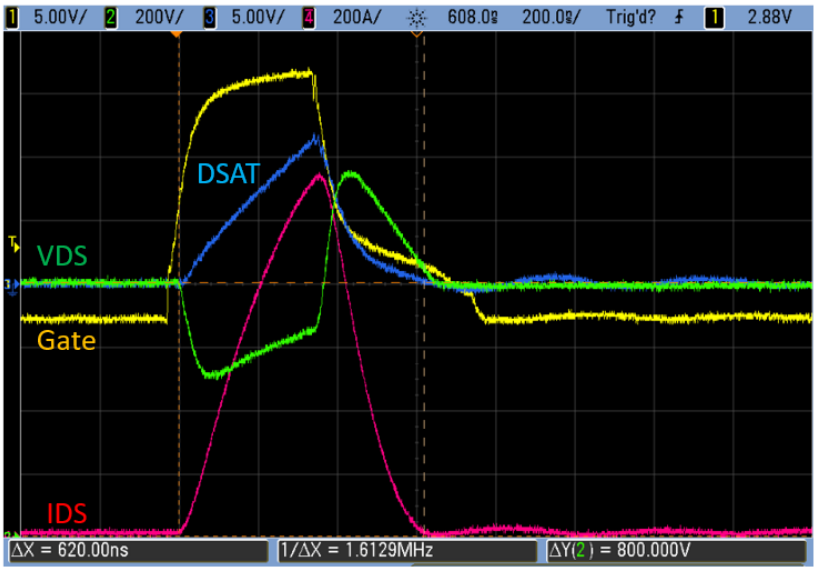


FIGURE 7: C3M0016120K SHORT CIRCUIT TEST WITH V_{BUS}=800V, R_{SS}=10

SiC MOSFET	V_{BUS}	R_G	R_{SS}	C_{BL} (pF)	RI (kΩ)	Detect Time (nS)	Soft Shutdown Time (nS)	I_{PK} (A)	V_{DS_PK} (V)	0A to 0A time (nS)
C3M0065100K	600	5	50	270	2.2	280	250	280	750	530
C3M0016120K	600	0	30	270	2.2	320	740	900	732	700
C3M0016120K	600	0	5	270	2.2	320	340	900	868	480
C3M0016120K	800	2.5	50	390	2.2	500	1100	1200	950	1200
C3M0016120K	800	2	50	270	2.2	340	1100	1150	950	1000
C3M0016120K	800	2	10	270	2.2	340	400	1150	1150	620

Table 3 below summarizes the short-circuit testing performed. It should be noted that in order to achieve a similar short-circuit duration for each of the SiC MOSFETs, a lower Rss is needed for the C2M0016120K due to the fact that it has a larger gate charge (211nC vs 37nC).

SiC MOSFET	V_{BUS}	R_G	R_{SS}	C_{BL} (pF)	RI (kΩ)	Detect Time (nS)	Soft Shutdown Time (nS)	I_{PK} (A)	V_{DS_PK} (V)	0A to 0A time (nS)
C3M0065100K	600	5	50	270	2.2	280	250	280	750	530
C3M0016120K	600	0	30	270	2.2	320	740	900	732	700
C3M0016120K	600	0	5	270	2.2	320	340	900	868	480
C3M0016120K	800	2.5	50	390	2.2	500	1100	1200	950	1200
C3M0016120K	800	2	50	270	2.2	340	1100	1150	950	1000
C3M0016120K	800	2	10	270	2.2	340	400	1150	1150	620

TABLE 3: SHORT CIRCUIT TEST RESULTS

3.2 Crosstalk Testing

Crosstalk or Miller turn-on may occur in a hard-switched topology and refers to an unintended turn-on event caused by the opposite device in a phase leg turning on. For example, when the top SiC MOSFET turns on, the V_{DS} of the lower SiC MOSFET experiences a high dv/dt as its drain is pulled up to +BUS. This dv/dt acts to charge the gate of the lower SiC MOSFET via the Miller capacitance (C_{GD}) pulling the gate voltage up. If the gate voltage is pulled too high, the device can turn on, creating a shoot-thru on the phase leg. Driving the SiC MOSFETs with a small negative gate bias (~-3V) and using a driver with a Miller clamp such as the Si828x will prevent false turn-ons. Additionally, adjusting the gate drive resistance to lower the dv/dt reduces this effect. While an increased gate resistance will increase switching losses, lowering the dv/dt will help meet EMC requirements and reduce ringing, so a balanced approach is necessary.

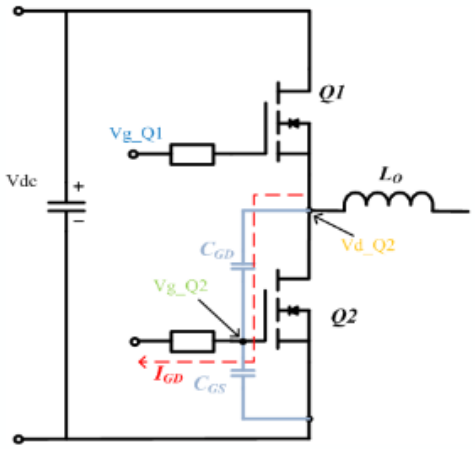


FIGURE 8: DIAGRAM SHOWING MILLER CAPACITANCE INDUCED GATE CHARGING CAUSED BY DV/DT OF THE SWITCHING NODE

Board Setup:

The board setup is similar to the set up for short-circuit testing, but with the shorting jumper removed. In this case, the bottom SiC MOSFET was gated off continuously, and the top SiC MOSFET was controlled by a function generator. The gate voltage of the lower SiC MOSFET was monitored at the time that the top SiC MOSFET was switched.

Test Results:

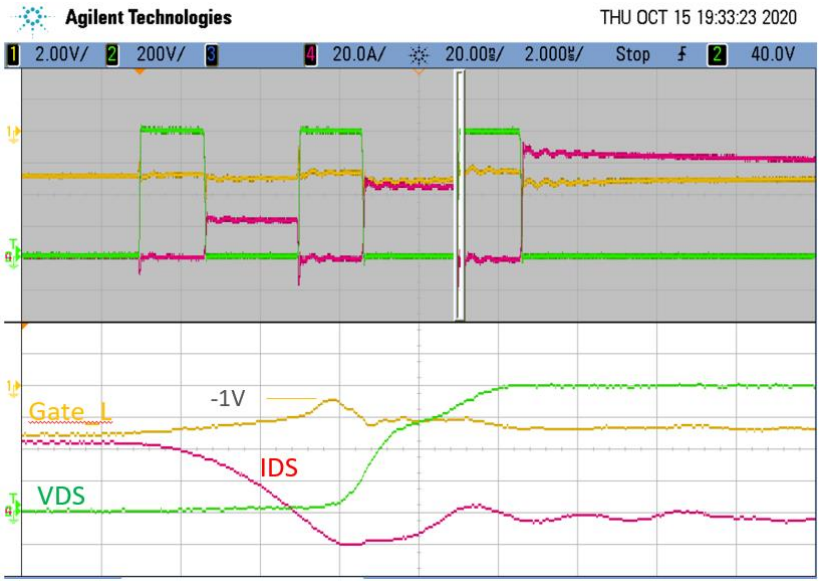


FIGURE 9: C3M0016120K WITH R_G=10OHMS, V_{DS}=800V

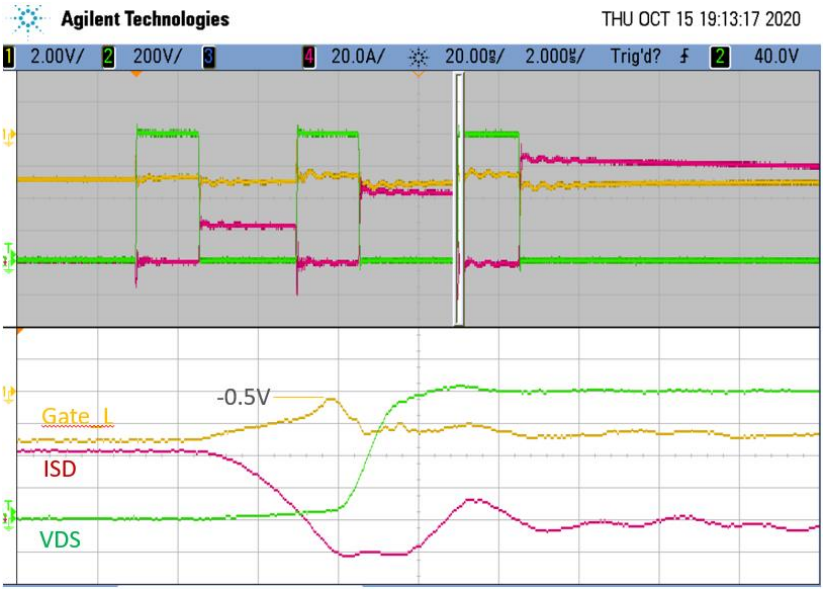


FIGURE 10: C3M0016120K WITH R_G=2.5OHMS, V_{DS}=800V

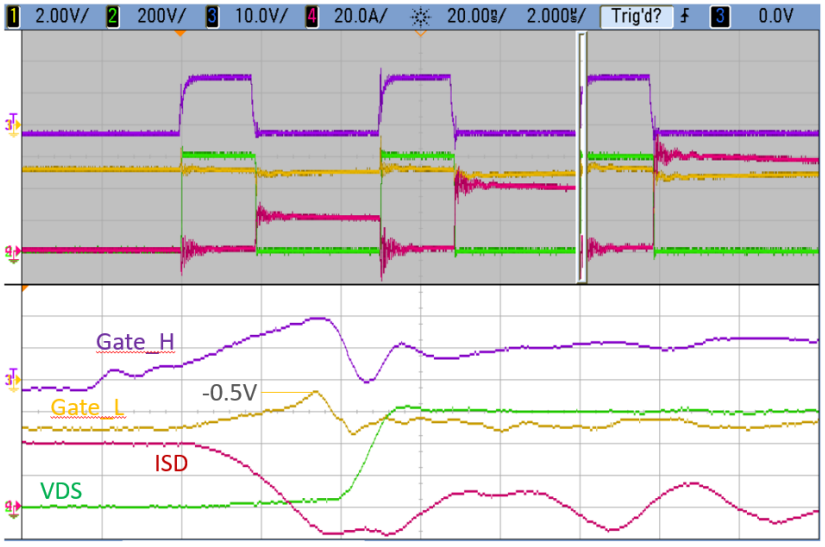


FIGURE 11: C3M0016120K WITH R_G=2OHMS, V_{DS}=600V

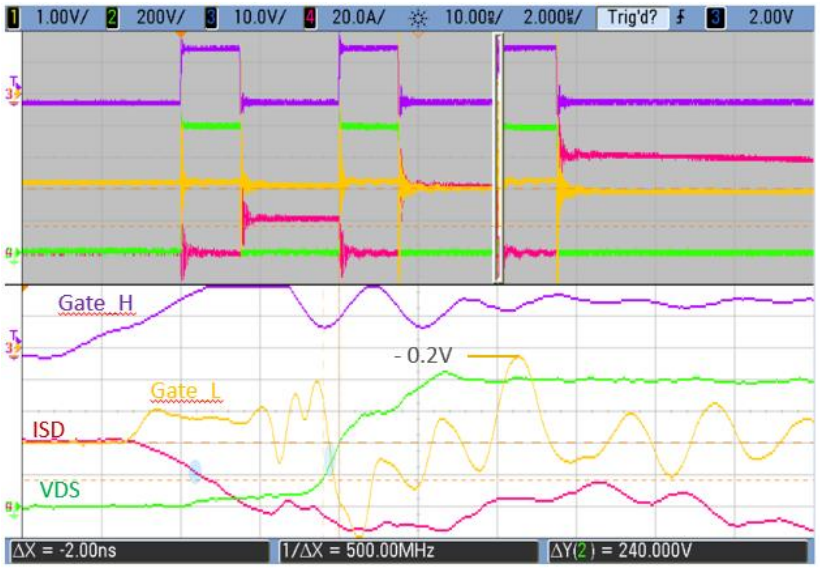


FIGURE 12: C3M0065100K WITH R_G=2OHMS, V_{DS}=800V

Table 4 below summarizes the crosstalk test data. It shows that even under the extreme condition of 120V/ns the driver can keep the SiC MOSFET safely turned off at -0.2V.

SiC MOSFET	V_{BUS}	R_G (Ω)	Switching Current (A)	dv/dt (V/ns)	V_G Max (V)
C3M0016120K	800	10	40	30	-1
C3M0016120K	800	2.5	40	55	-0.5
C3M0016120K	600	2	40	60	-0.5
C3M0065100K	800	2	40	120	-0.2

TABLE 4: CROSSTALK TEST RESULTS

Power 3.3 Switching Loss Testing

Switching loss testing was performed to verify that the gate driver has sufficient current source and sink capability to drive the SiC MOSFETs appropriately.

Board Setup:

A DC power supply was connected to the bus, and an air-core inductor was connected across the upper SiC MOSFET. A function generator was used to provide a short burst of gate pulses to the lower SiC MOSFET. The upper SiC MOSFET was held off for this testing, allowing the body diode to operate during the lower SiC MOSFET off-time. The current in the inductor ramped up during the lower SiC MOSFET on-time and freewheeled through the upper SiC MOSFET body diode during the off-time. Turn-on and turn-off switching losses were measured at the lower SiC MOSFET at several different current levels.

Scope Setup:

A 10x passive probe was connected across the lower SiC MOSFET gate-source connection using an SMA to BNC adapter. A current viewing resistor was inserted in the source path of the lower SiC MOSFET to measure current in that device. A 100x passive probe was connected across the lower SiC MOSFET drain-source. The probe ground wire was kept as short as possible and wrapped around the probe tip to minimize the loop area of the probe.

Switching Energy Measurements:

The switching energy measurements were taken by multiplying voltage across the drain and source (VDS) and the current through the device (IDS) during the turn-on and turn-off event. The product of VDS and IDS yields the switching power waveform (purple). To measure the switching energy, you simply take the area underneath the power curve (purple) during turn-off or turn-on. The two channels being multiplied must be de-skewed to yield accurate measurements.

FIGURE 13: EXAMPLE OF TURN OFF WAVEFORMS

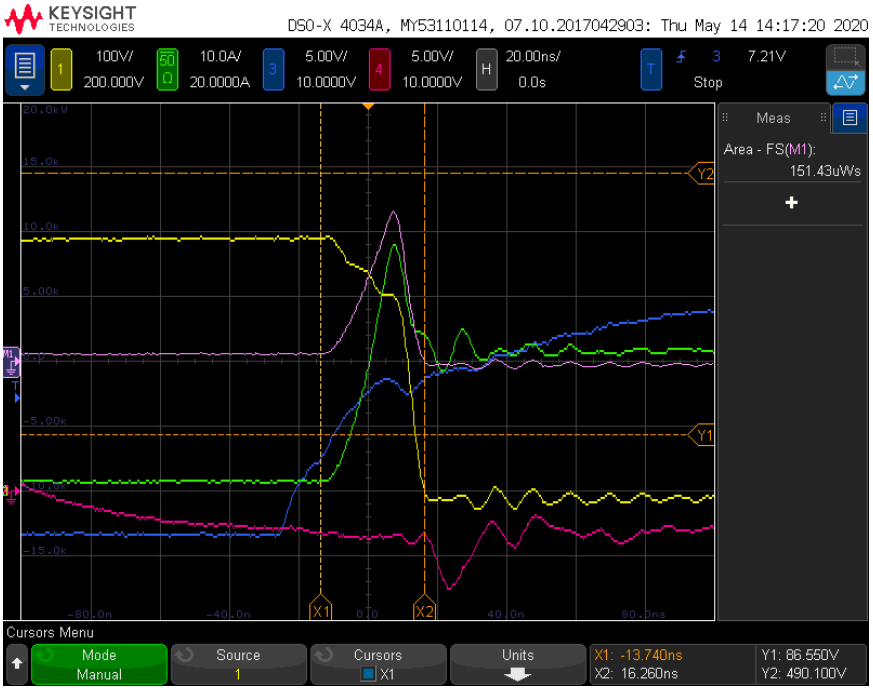


FIGURE 14: EXAMPLE OF TURN ON WAVEFORMS

Test Results - C3M0065100K:

The C3M0065100K part was characterized with a 600V bus at approximately 20C with three different gate resistor values.

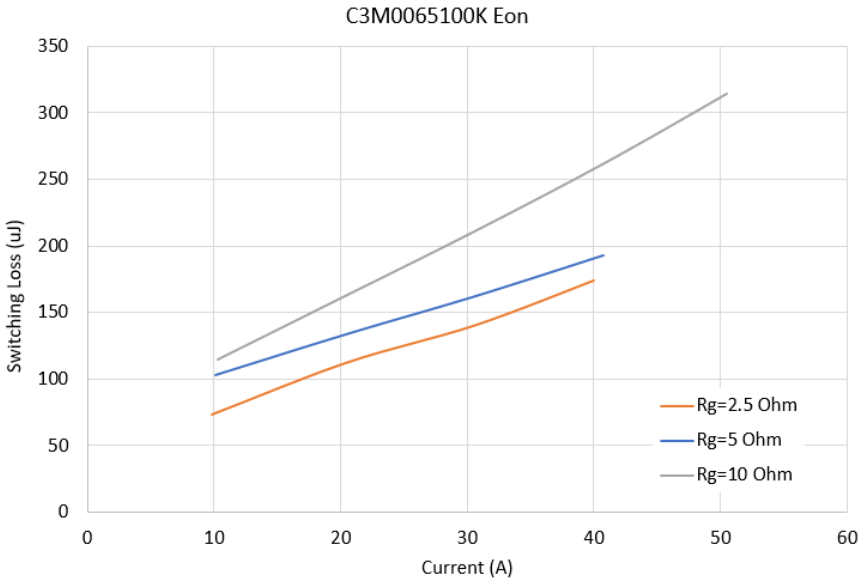


FIGURE 15: TURN-ON SWITCHING LOSS DATA FOR C3M0065100K WITH DIFFERENT GATE RESISTORS

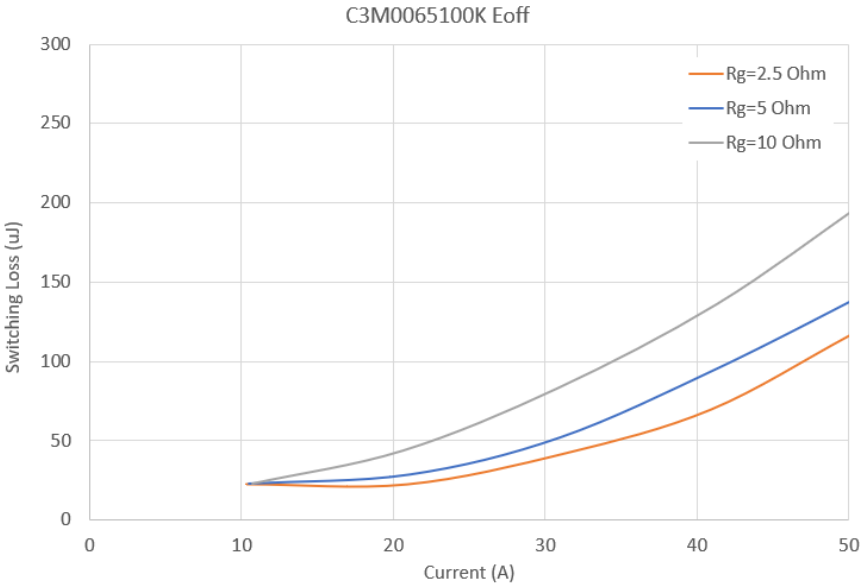


FIGURE 16: TURN-OFF SWITCHING LOSS DATA FOR C3M0065100K WITH DIFFERENT GATE RESISTORS

Test Results - C3M0016120K:

The C3M0016120K part was characterized with an 800V bus at approximately 20C with two different gate resistor values.

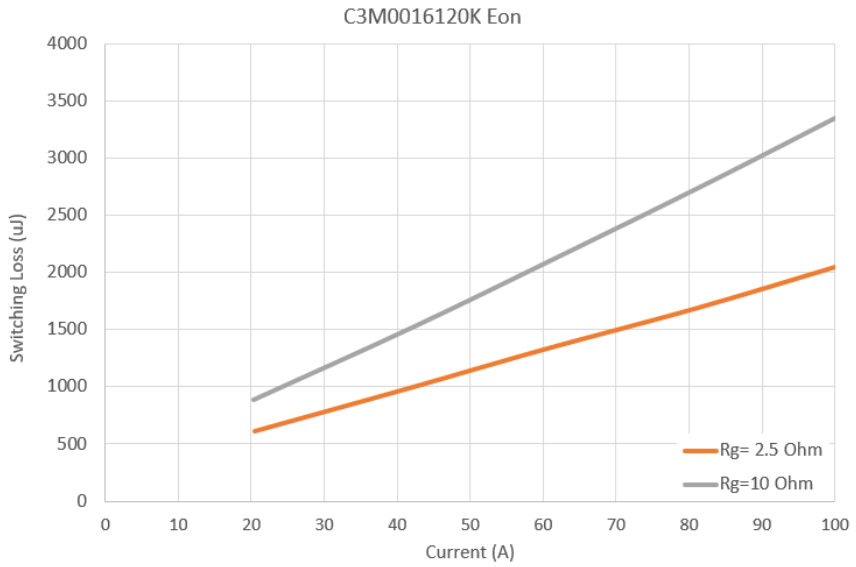


FIGURE 17: TURN-ON SWITCHING LOSS DATA FOR C3M0016120K WITH DIFFERENT GATE RESISTORS

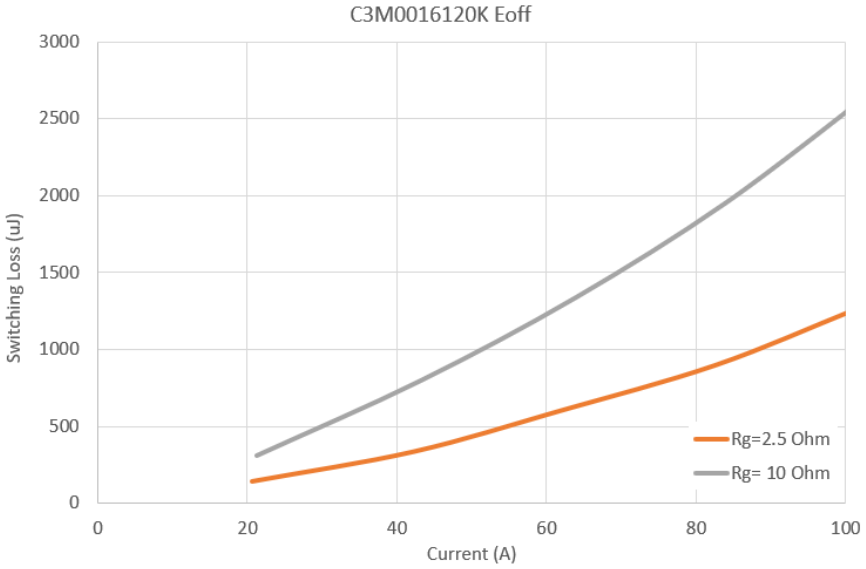


FIGURE 18: TURN-OFF SWITCHING LOSS DATA FOR C3M0016120K WITH DIFFERENT GATE RESISTORS

These results demonstrate the effect of different gate resistances on the switching losses and confirm that the gate driver is able drive the SiC MOSFETs with a low, 2.5-ohm gate resistor.

3.4 Operational Testing

The evaluation board was setup to run as a synchronous boost converter to demonstrate the high efficiency of the SiC MOSFETs and the robustness of the gate driver in a hard-switched high-power converter. The evaluation board was modified thermally for this experiment to enable higher power testing, but the electrical circuits were unchanged.

Board Setup:

A heatsink and fan were added to the SiC MOSFETs to facilitate high-power testing. Additionally, an off-board boost inductor was utilized to allow for higher power testing than the on-board part. A high voltage DC supply from Magna-Power (P/N TSD800-54/480+LXI) provided the input power to the board and a DC electronic load from Elektro-Automatik (P/N EA-ELR 11500-60) was used to pull power from the boosted bus. A two-channel signal generator was used to create out-of-phase 60kHz PWM commands for the gates running at 48.5% duty cycle.

Efficiency measurements:

Efficiency measurements were taken with a Yokogawa® (P/N WT1806E) Precision Power Analyzer. Voltages were taken directly from the input and output terminals of the evaluation board.

FIGURE 19: EQUIPMENT USED FOR OPERATIONAL TESTING

Thermal Measurements:

All thermal measurements were taken with a FLIR (P/N T420) infrared camera like the one shown below.

FIGURE 20: THERMAL CAMERA USED FOR MEASUREMENTS

Test Results - C3M0016120K:

Table 5 shows the results running Cree C3M0016120K SiC MOSFETs with a 2.5ohm gate resistor. The circuit was configured with a 400V input and approximately 785V of output.

Pout (KW)	Efficiency	Upper SiC MOSFET Case (°C)	Lower SiC MOSFET Case (°C)	Upper Gate Driver Case (°C)	Lower Gate Driver Case (°C)
2.0	98.37%	29.0	42.9	32.4	30.9
3.0	98.79%	30.1	45.9	32.4	30.7
4.0	98.95%	32.3	50.0	33.2	31.3
6.0	99.01%	35.6	56.4	32.8	30.7
8.0	99.03%	40.3	65.1	33.3	30.7
10.0	98.98%	46.9	76.6	34.9	32.0

TABLE 5: EFFICIENCY AND THERMAL RESULTS USING C3M0016120K SIC MOSFETS

Table 6 shows the measured dv/dt and di/dt at the 10kW operating point.

	Turn On		Turn off	
Power (kW)	dv/dt (V/ns)	di/dt (A/ns)	dv/dt (V/ns)	di/dt (A/ns)
10.0	42.8	2.47	28.7	0.937

TABLE 6: C3M0016120K DV/DT AND DI/DT

Test Results - C3M0065100K:

Table 7 shows the results running Cree C3M0065100K SiC MOSFETs with a 2.5ohm gate resistor. The circuit was configured with a 300V input and approximately 590V of output.

Pout (KW)	Efficiency	Upper SiC MOSFET Case (°C)	Lower SiC MOSFET Case (°C)	Upper Gate Driver Case (°C)	Lower Gate Driver Case (°C)
1.0	98.65%	27.90	32.80	28.40	30.00
2.0	99.13%	31.00	36.40	28.60	30.30
3.0	99.19%	35.10	41.70	29.30	30.80
4.0	99.11%	39.80	48.30	29.50	30.90
6.0	98.93%	53.40	67.30	29.90	30.80
8.0	98.55%	83.60	108.10	31.80	31.50

TABLE 7: EFFICIENCY AND THERMAL RESULTS USING C3M0065100K SIC MOSFETS

Table 8 shows the measured dv/dt and di/dt at the 8kW operating point.

	Turn On		Turn off	
Power (kW)	dv/dt (V/ns)	di/dt (A/ns)	dv/dt (V/ns)	di/dt (A/ns)
8.0	41.3	5.79	118	3.41

TABLE 8: C3M0065100K DV/DT AND DI/DT

4. Conclusion

The Si828x family of gate drivers from Silicon Labs was demonstrated in the tests described above to perform well in a hard-switched topology requiring short-circuit protection. The driver can detect a short circuit condition and turn off the SiC MOSFET in a controlled manner using the soft-shutdown feature. This protects the SiC MOSFET from damage due to overcurrent and reduces voltage overshoot.

The Silicon Labs' Si828x driver was tested with each of Cree's 1200V (P/N C3M0016120K) and 1000V (P/N C3M00651000K) SiC discrete MOSFETs and demonstrated sufficient drive strength to switch the parts quickly, minimizing the switching loss. Furthermore, it demonstrated immunity to both crosstalk and high common-mode transients present in a hard-switched SiC MOSFET application. The Miller Clamp and negative gate bias eliminates a dv/dt induced turn-on in a hard-switched topology.

Together Silicon Lab's Si828x family of drivers and Cree's 3rd Generation SiC MOSFETs identified in this report enable high-efficiency and robust power converters.