Design Models

How to Use LTspice® Models

ROHM provides the LTspice models for simulating electrical circuits. This application note explains how to add models to LTspice.

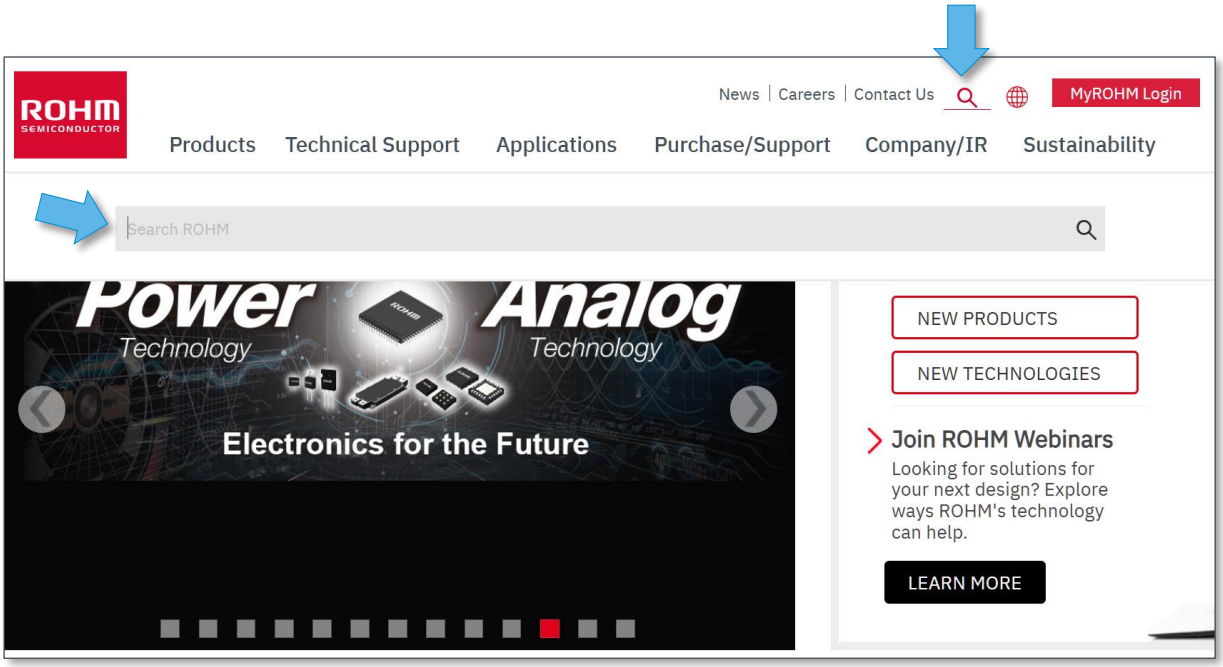
Contents

LTspice® is a registered trademark of Analog Devices, Inc.

1. How to obtain the models

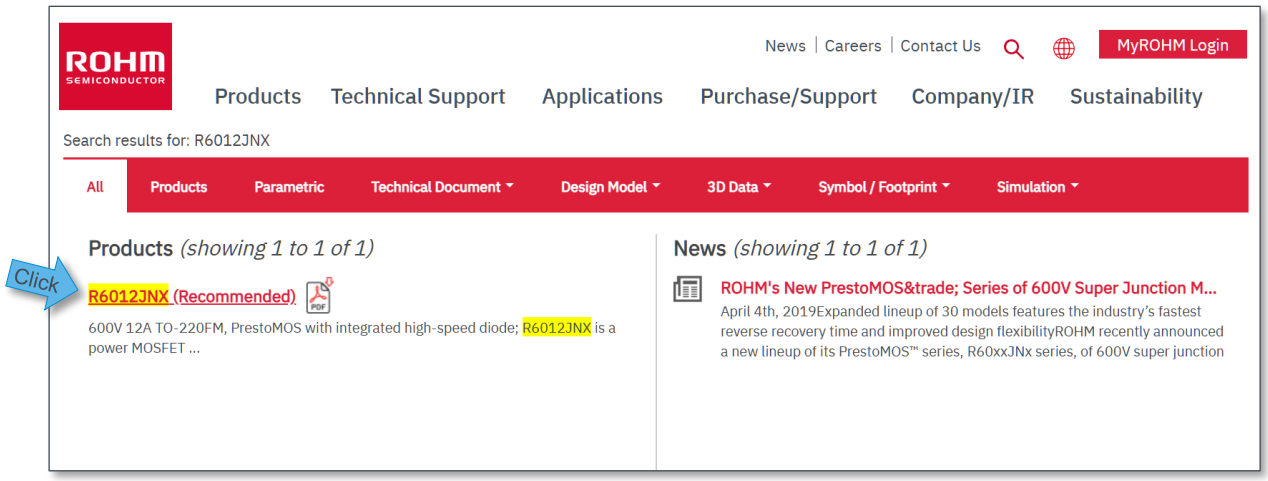
Step 1

- Access the ROHM website. Enter the product model name in the “Search ROHM” box on the upper right of the home page.



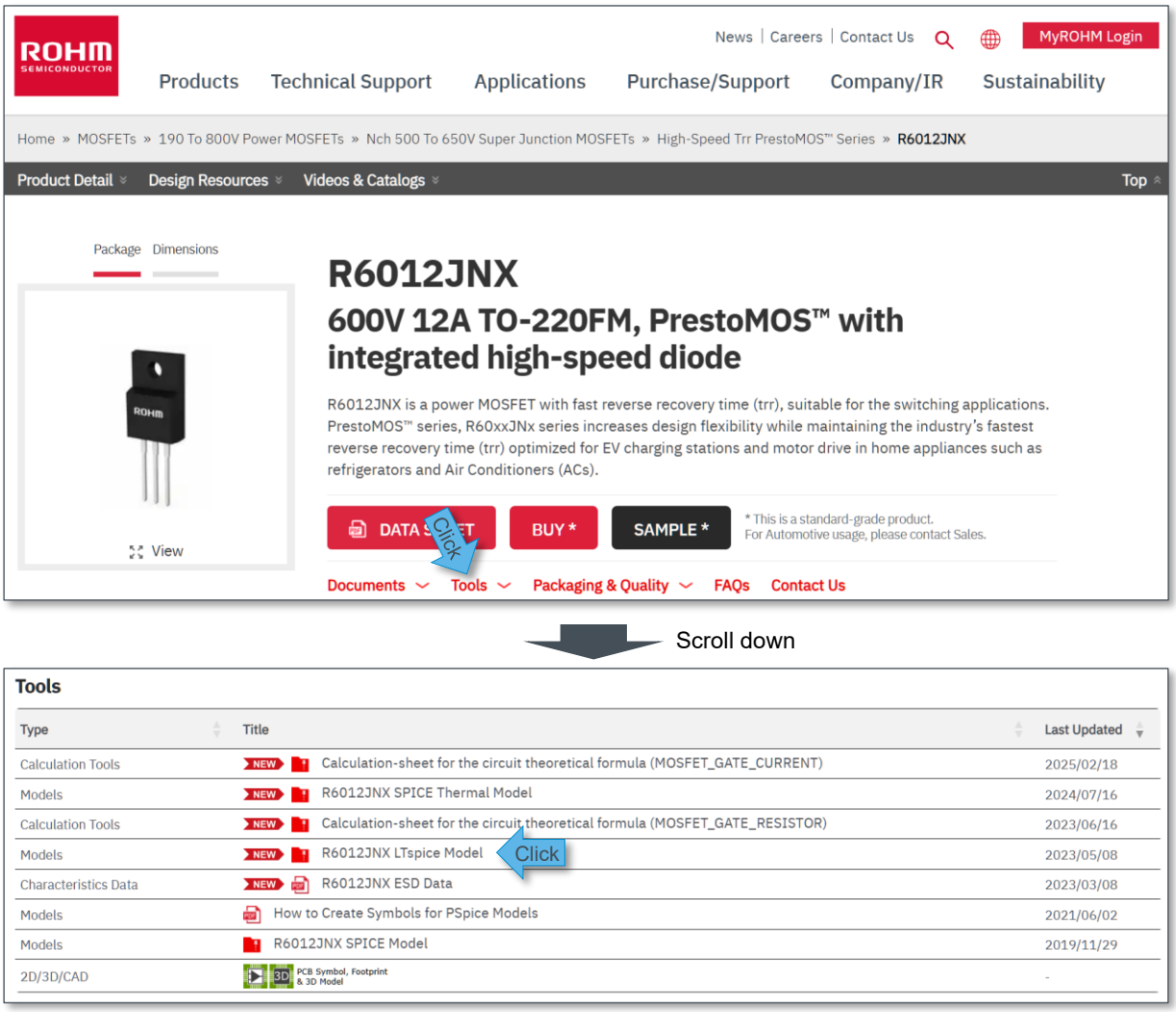
Step 2

- Click on the applicable model name in the search results.



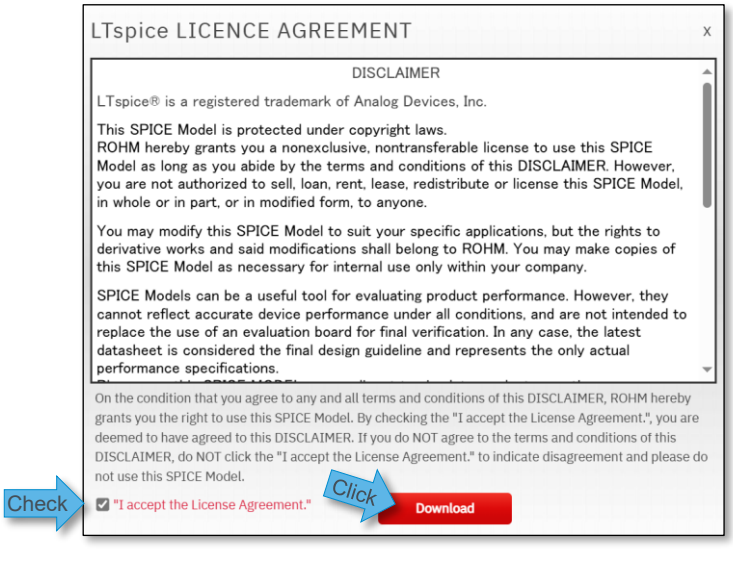
Step 3

- When the product page is displayed, click “Tools”.
- Scroll down to “Tools”, locate and click the LTspice model.



Step 4

- When “LICENCE AGREEMENT” is displayed, check “I accept the License Agreement.” and click “Download” to download the file.



2. Model types

The models are classified into two types: device model and subcircuit model. You can check the syntax by opening the downloaded file with a text editor. The device models cover single elements, including bipolar transistors and diodes. The syntax starts with ".MODEL". The subcircuit models cover configurations with multiple elements, including MOSFET, SiC power devices, and IGBT. The syntax starts with ".SUBCKT" and ends with ".ENDS". Among the subcircuit models, the models for MOSFET are described as macro models representing MOSFET with equivalent circuits configured with the passive and active elements and the power supply. As a result, there are multiple ".MODEL". SiC power devices and IGBT are described as behavior models representing the device characteristics with specific numerical expressions.

<table>
<tr><td>Model types</td><td>Device model</td><td colspan="2">Subcircuit model</td></tr>
<tr><td>First command</td><td>.MODEL</td><td colspan="2">.SUBCKT</td></tr>
<tr><td>Main devices</td><td>Bipolar transistor
Diode
LED</td><td colspan="2">MOSFET (macro model)
Some Zener diode (behavior model)
Some TVS diode (macro model, behavior model)
SiC power device (behavior model)
GaN power device (behavior model)
IGBT (behavior model)
Bi-directional TVS diode (macro model)
Digital Transistor (macro model)
Darlington Transistor (macro model)
Complex Transistor (macro model)
Laser Diode (behavior model)</td></tr>
<tr><td>Syntax examples</td><td>

```
* Q2SC4081UB NPN BJT model
* Date: 2006/11/30
.MODEL Q2SC4081UB NPN
+ IS=70.000E-15
+ BF=277.08
+ VAF=114.03
+ IKF=1
+ ISE=70.000E-15
+ NE=1.8934
+ BR=11.565
+ VAR=100
+ IKR=.11266
+ ISC=1.0228E-12
+ NC=1.3260
+ NK=.71869
+ RE=.2
+ RB=13.897
+ RC=1.2190
+ CJE=11.342E-12
+ MJE=.38289
+ CJC=4.0230E-12
+ MJC=.34629
+ TF=338.92E-12
+ XTF=4.0449
+ VTF=167.36
+ ITF=.85959
+ TR=110.25E-9
+ XTB=1.5000
```

</td><td>Macro model

```
* R6006JNX NMOSFET model
* PKG: TO-220FM,Vdss=600V,Id=6A
* Rds(on)=0.72Ω,Qg=15.5nC
* Model Generated by ROHM
* All Rights Reserved
* Date: 2017/07/27
*****************D G S
.SUBCKT R6006JNX 1 2 3
M1   11 22 3 3 MOS_N
D1         3 1 DDS
R1        1 11 RTH 697.2m
D2       22 11 DDG
R2        2 22 14.8
.MODEL MOS_N NMOS
+ LEVEL=3
+ L=2.0000E-6
+ W=1
     : (omitted)
+ KAPPA=0
+ NFS=36G
.MODEL DDS D
+ IS=2.2476E-6
+ N=2.1699
     : (omitted)
+ BV=600
+ TT=70n
.MODEL DDG D
+ CJO=172.09E-12
+ M=3.3976
     : (omitted)
+ FC=0.11
+ T_ABS=25
.MODEL RTH RES
+ TC1=0.0073
+ TC2=0.0200E-3
.ENDS R6006JNX
```

</td><td>Behavior model

```
* SCT4018KR SiC NMOSFET model
* TO247-4L
* 1200V 90A 18mOhm
* Model Generated by ROHM
* All Rights Reserved
* DATE:2022/02/03
*****************D G S DS
.SUBCKT SCT4018KR 1 2 3 4
.PARAM T0=25
*
.FUNC R1(I)
{18.49m*I*EXP((TEMP-T0)/207.9*EXP((TE
MP-T0)/880))+905.2n*I*ABS(I)**1.745*E
XP((TEMP-T0)/160.2*EXP((TEMP-T0)/348.
4))}
.FUNC R2(I)
{5*MAX(I,0)+5*MIN(I,0)}
.FUNC V1(V,W)
{V-67.95m*ASINH(W/17.87m)*EXP((TEMP-T
0)/-323.4)-270.9m*ASINH(W/693.3m)*EXP
((TEMP-T0)/-260.5)-43.83m*W*EXP((TEMP
-T0)/3.368k)}
     :
     : (omitted)
     :
V12 52 53 0
C11 53  1 1p
G11 52  1
VALUE={I11(MIN(MAX(V(52,1),-4.5k),3.6
))+I(V12)*C11(MAX(V(52,1),625.6m),MIN
(V(52,1),625.6m))}
R11 52  1 1T
.ENDS SCT4018KR
```

</td></tr>
</table>

3. File configuration of LTspice

When LTspice is installed, files are created in the configuration as shown in Figure 1. The folders related to the model and symbol files are \cmp, \sub, and \sym under \LTspice\lib. Folder \cmp stores the standard parts libraries, which are created with the device models. Folder \sub stores the libraries other than those for the standard parts, which are mainly created with the subcircuit models. Naturally, it can also store the device models. Folder \sym stores the circuit diagram symbol files. The model files in folder \sub and the circuit diagram symbol files (.asy) in folder \sym are linked so that they can be used on circuit diagrams.

In the following, we explain several ways for adding the models. Remember the configuration of these folders because the storage folder depends on the method used to add device models.

C:\Users\%USERNAME%\AppData\Local\LTspice\lib

- \cmp : Stores the standard parts libraries (device models)
  - \standard.bead : Ferrite bead
  - \standard.bjt : Bipolar transistor
  - \standard.cap : Capacitor
  - \standard.dio : Diode
  - \standard.ind : Inductor
  - \standard.jft : JFET
  - \standard.mos : MOSFET
  - \standard.res : Resistor
- \sub : Stores the libraries other than those described above (subcircuit and device models)
  - \xxxxxxxx.sub : sub file
  - \xxxxxxxx.lib : lib file
- \sym : Stores the circuit diagram symbol files
  - \xxxxxxxx.asy : Circuit diagram symbol

Figure 1. Folder configuration and libraries of LTspice

Device Models

4. Confirming the device models

For ROHM's product, the device models of bipolar transistors, diodes, and LED are provided. Open the downloaded model file with a text editor and confirm that the syntax starts with ".MODEL".

5. How to add the device models

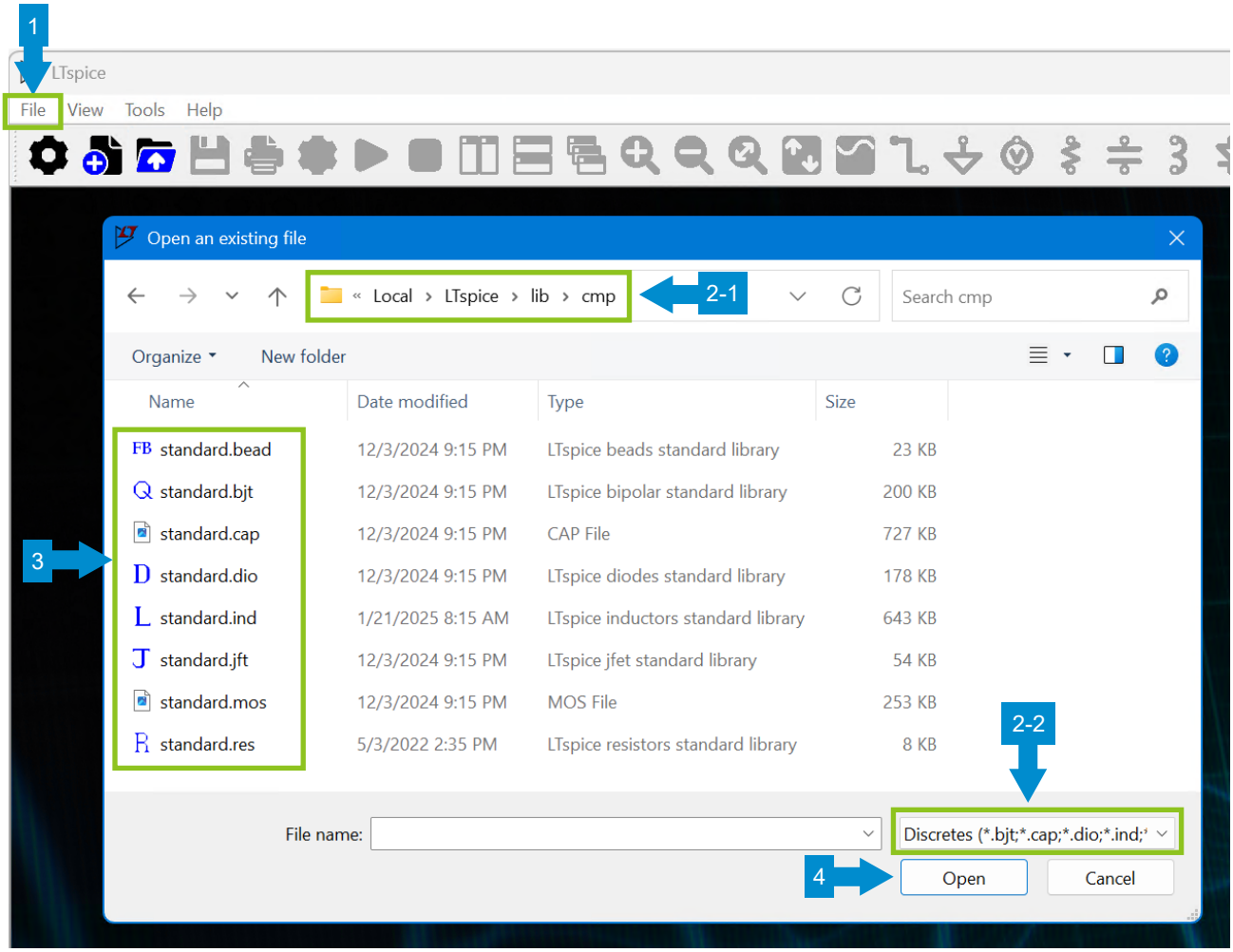
We explain three methods to add device models here. Since each method has advantages and disadvantages, select the method most suited for your application.

	Method 1 Add the model to the standard parts library of LTspice	Method 2 Describe the model information on the circuit diagram	Method 3 Store the model in a desired parts folder
Outline of the procedure	1. Open the standard library 2. Copy the model file to be added to the standard library in text format 3. Place the symbol on the circuit diagram 4. Select the model from the parts list	1. Place the symbol on the circuit diagram 2. Copy the model file to be added to "SPICE directive" in text format 3. Place the model text on the circuit diagram 4. Change the attribute of the symbol	1. Store the model file to be added 2. Place the symbol on the circuit diagram 3. Change the model name of the symbol 4. Write the command to read the ".lib" file in the circuit diagram
Advantages	- Can be selected from the parts list	- Since the parameters of the parts are displayed on the circuit diagram, the evidence of simulation can be checked with the circuit diagram only - Since simulations can be performed with the circuit diagram data only, they are independent of the PC environment	- Easy to manage the parts because they can be classified using folders
Disadvantages	- Reinstalling LTspice will overwrite the standard library, deleting the added models	- Many characters on the circuit diagram - Necessary to manage the parameters of the parts for each circuit diagram	- Necessary to redo the environment setting of the model files if the PC environment changes

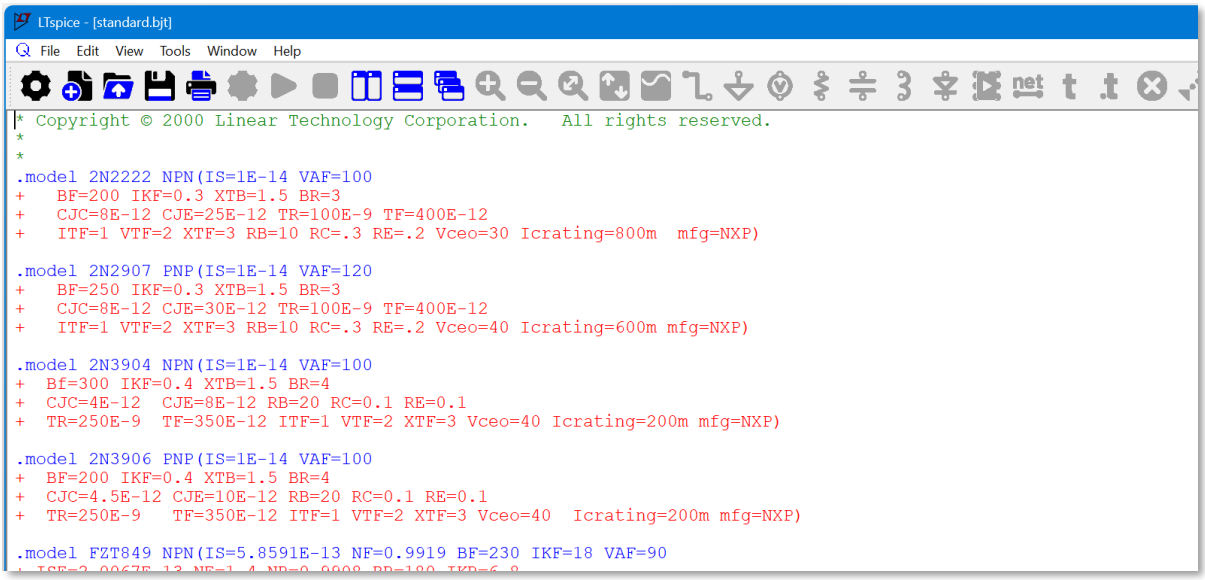
In the following, we explain the procedure in more detail for each method.

5-1. Method 1: Add the model to the standard parts library of LTspice

1. Click “File” and then “Open”.
2. When the “Open an existing file” window is displayed, move to “`C:\Users\%USERNAME%\AppData\Local\LTspice\lib\cmp`”. Select “Discretes” for the file type.
3. Select one of the following files corresponding to the part to be added. In this example, the NPN transistor model “2sc4081ub.lib” is added.
   - Bipolar transistor: standard.bjt
   - Diode: standard.dio
   - LED: standard.dio
4. Click “Open”.



5. “standard.bjt” is opened.

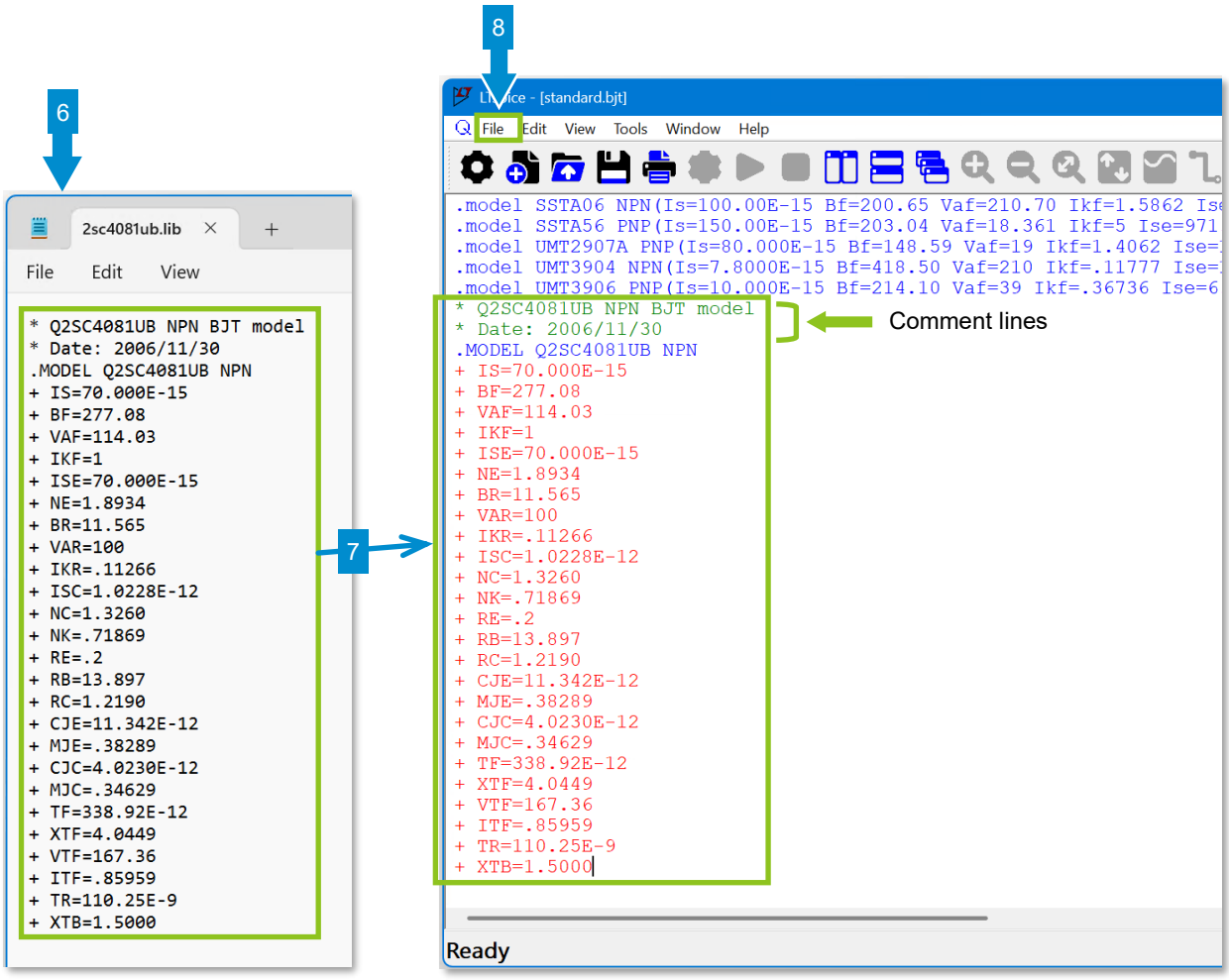


6. Open the model to be added with a text editor (e.g. Notepad).

7. Copy the contents to the last line of “standard.bjt”. At this time, you may delete unnecessary comment lines.

8. Click “File” and then “Save” to save changes. The model is now added.

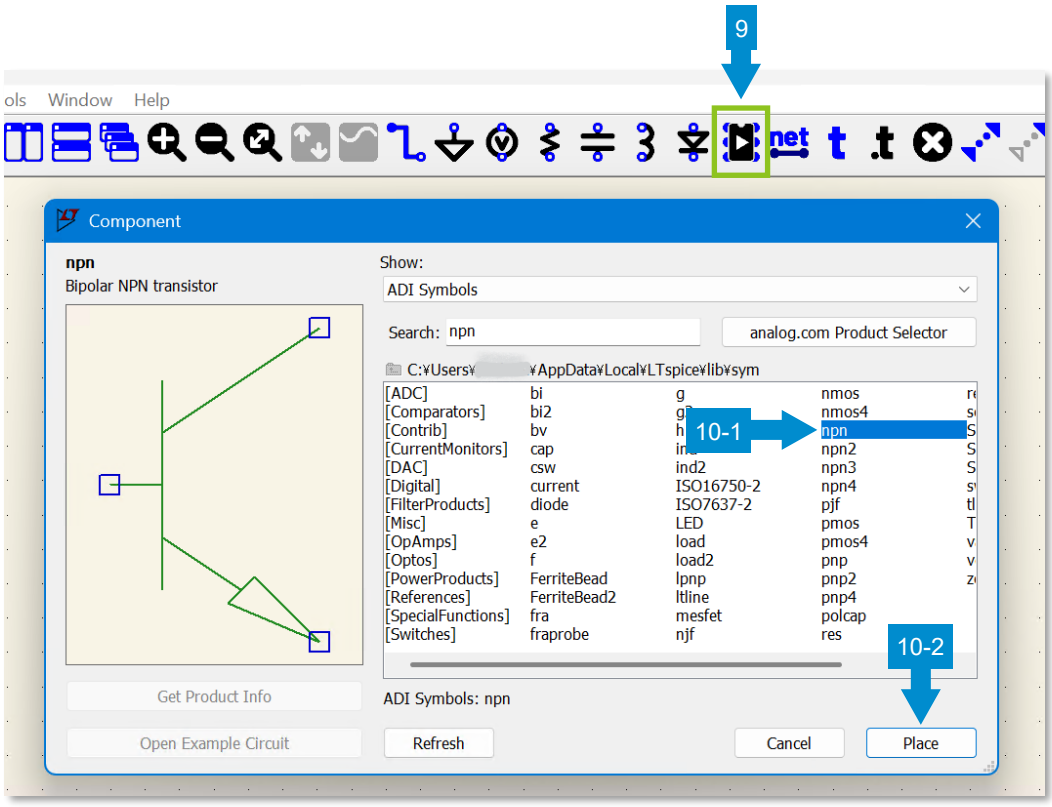
   Note: Files in this folder may be overwritten or removed when LTspice component libraries are updated. Files should be backed up before updating.



Next, place the transistor on the circuit diagram.

9. On the toolbar, click the “Component” icon to open “Component select window”.

10. From the list, select “npn” and then click “Place”. Select “pnp” for a PNP transistor, “diode” for a diode, and “LED” for an LED.

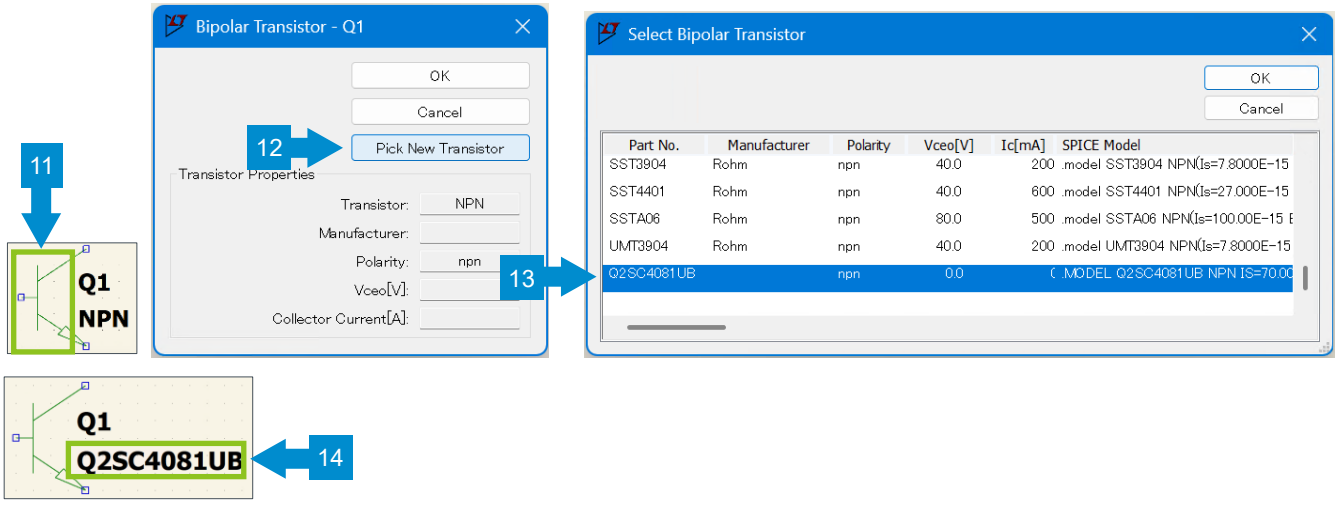


11. After placing the component on the circuit diagram, right-click on it.

12. When the property window is opened, click “Pick New Transistor”.

13. When the “Select Bipolar Transistor” window is opened, select “Part No.” for the component added above.

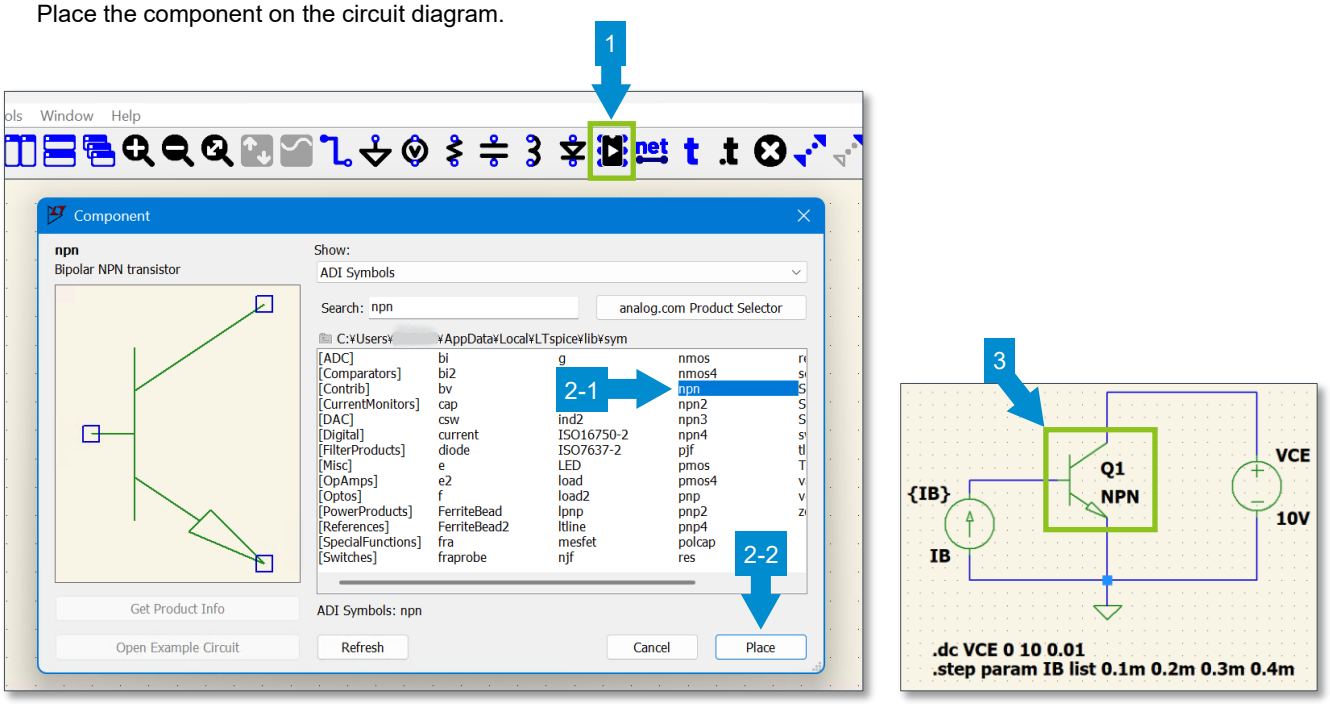
14. The model name on the circuit diagram is changed. This completes the setting.



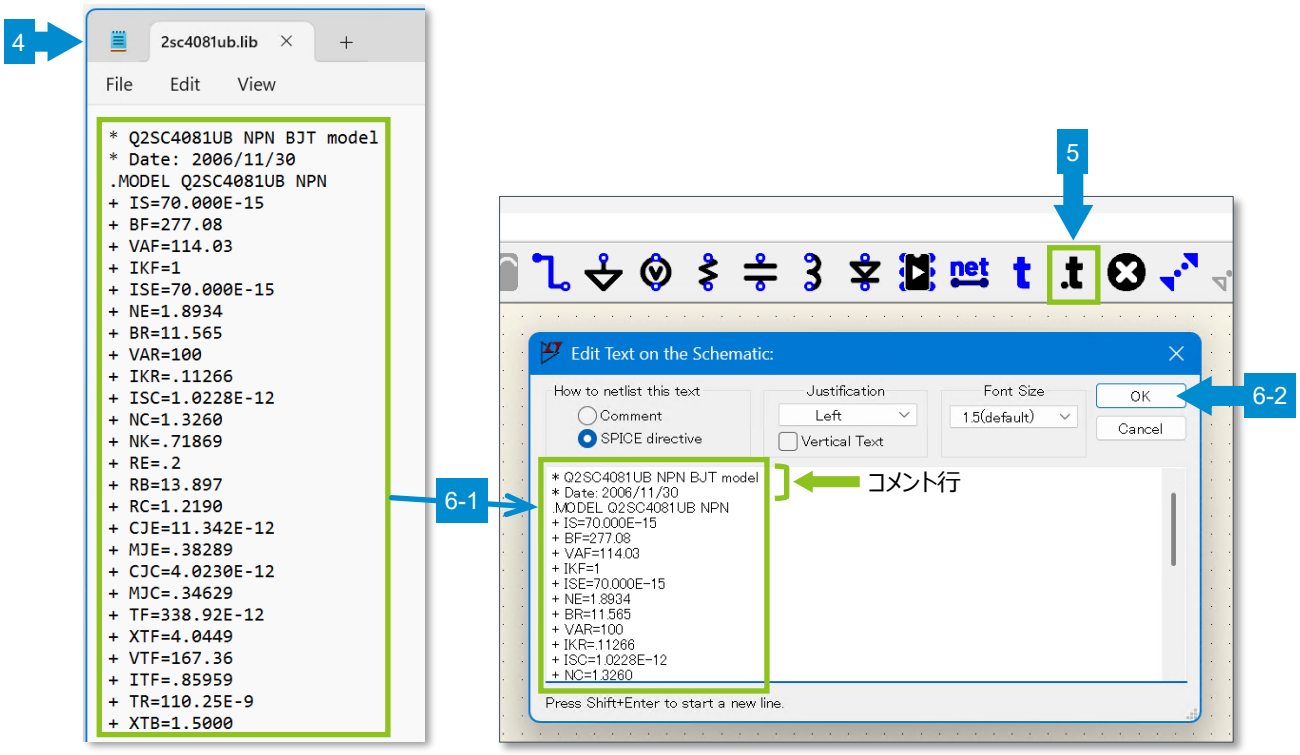
5-2. Method 2: Describe the model information on the circuit diagram

In this example, the NPN transistor model “2sc4081ub.lib” is added.

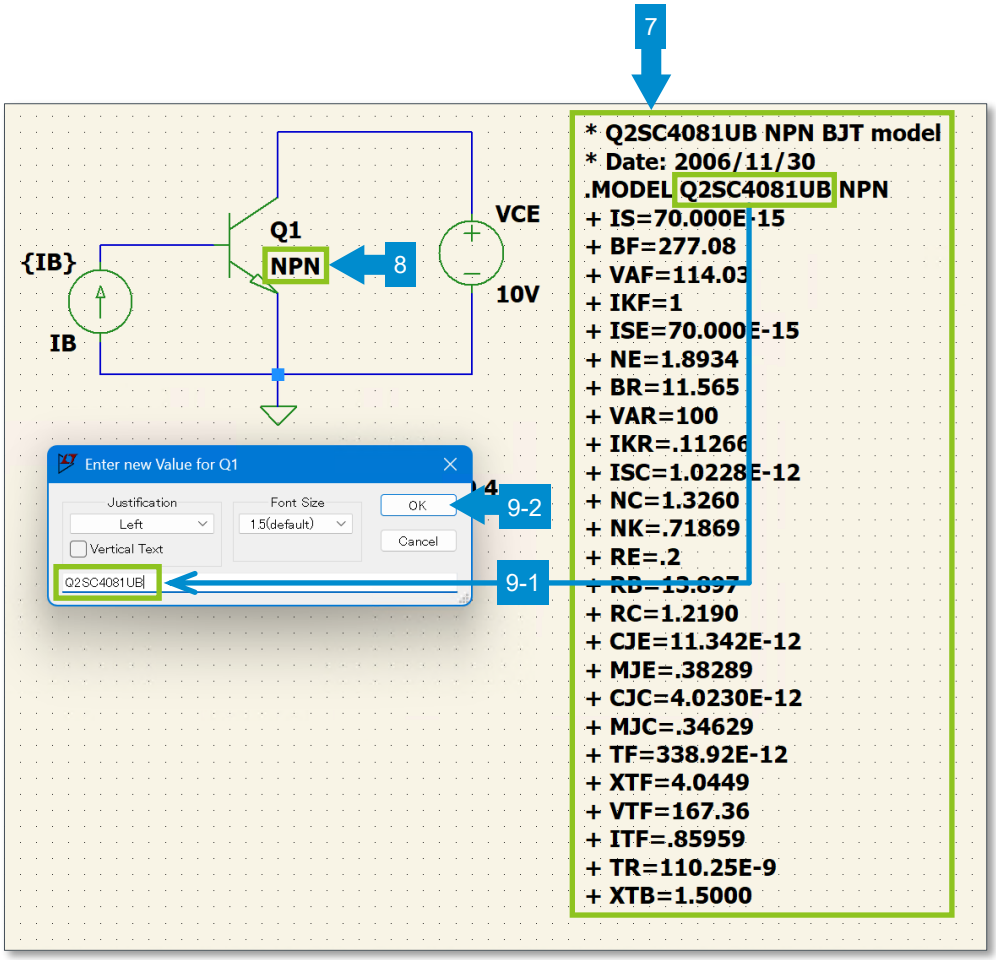
1. First, place the transistor on the circuit diagram. On the toolbar, click the “Component” icon to open “Component select window”.
2. From the list, select “npn” and then click “OK”. Select “pnp” for a PNP transistor, “diode” for a diode, and “LED” for an LED.
3. Place the component on the circuit diagram.

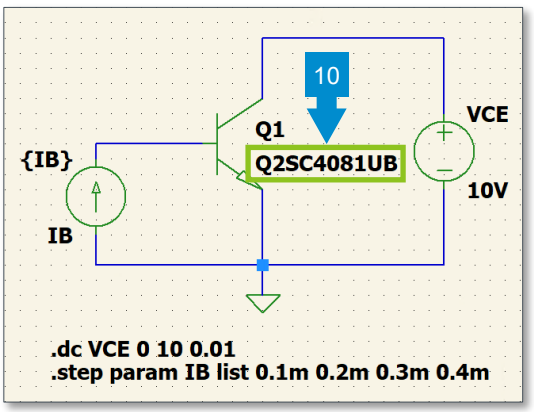


4. Open the model to be added with a text editor (e.g. Notepad).
5. On the toolbar, click “SPICE Directive” to open the input window.
6. Copy the contents of the model and then click “OK”. At this time, you may delete unnecessary comment lines.



7. Place the model text at an appropriate location on the circuit diagram.
8. Right-click on “NPN” of the transistor.
9. When the input window is opened, rename “NPN” with the model name and then click “OK”.
10. The model name on the circuit diagram is changed. This completes the setting.





5-3. Method 3: Store the model in a desired parts folder

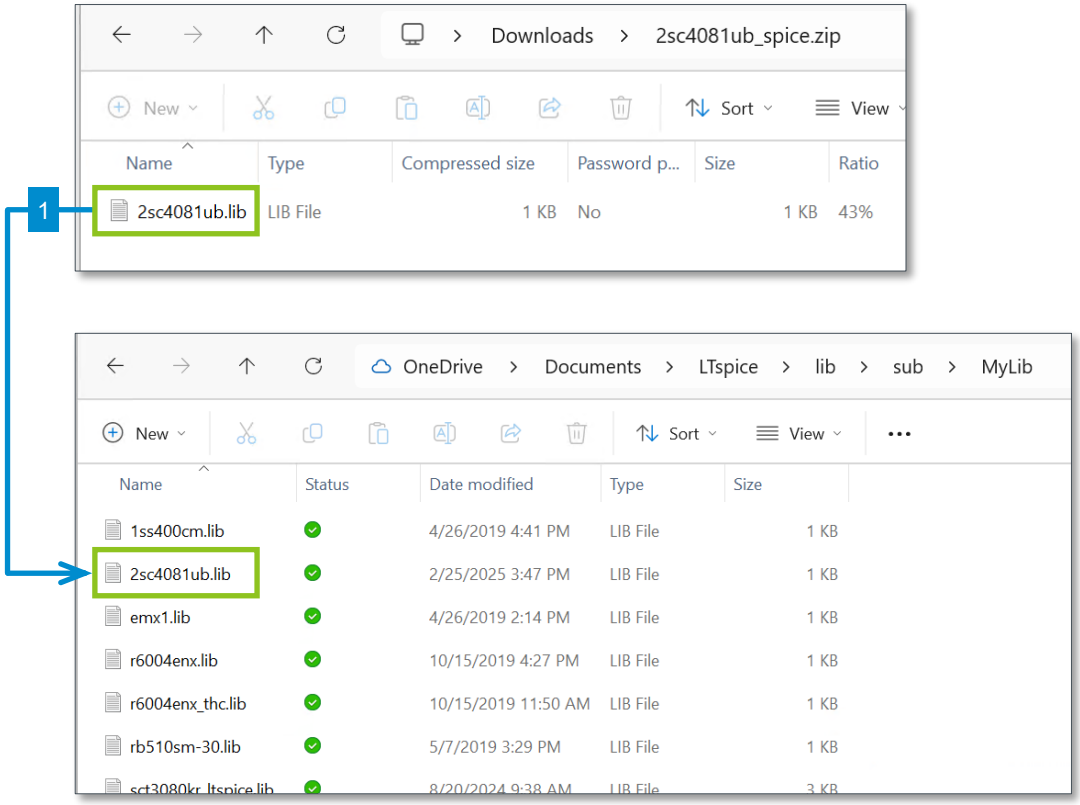
To distinguish the added models from the models installed as standard, you can create any folder and store the added models there. You can also store the added models in the same folder as the circuit diagram. In this way, you can store and use the models in a location where it is easy to manage them.

Examples of folders to store the models

a. LTspice Application Data folder : `C:\Users\%USERNAME%\AppData\Local\LTspice\lib\sub`
*This is not recommended. Files in this folder may be overwritten or removed when LTspice component libraries are updated.
b. Same folder as the circuit diagram : `D:\project-a\test_circuit` ← example
c. Any folder : `C:\Users\%USERNAME%\Documents\LTspice\lib\sub\MyLib` ← example
: `C:\Users\%USERNAME%\Documents\LTspice\lib\sub\ROHM` ←e.g., company name
: `E:\LTspicemodel\transistor\ROHM` ← example

As an example, we use a case where the NPN transistor model “2sc4081ub.lib” is stored in an any folder.

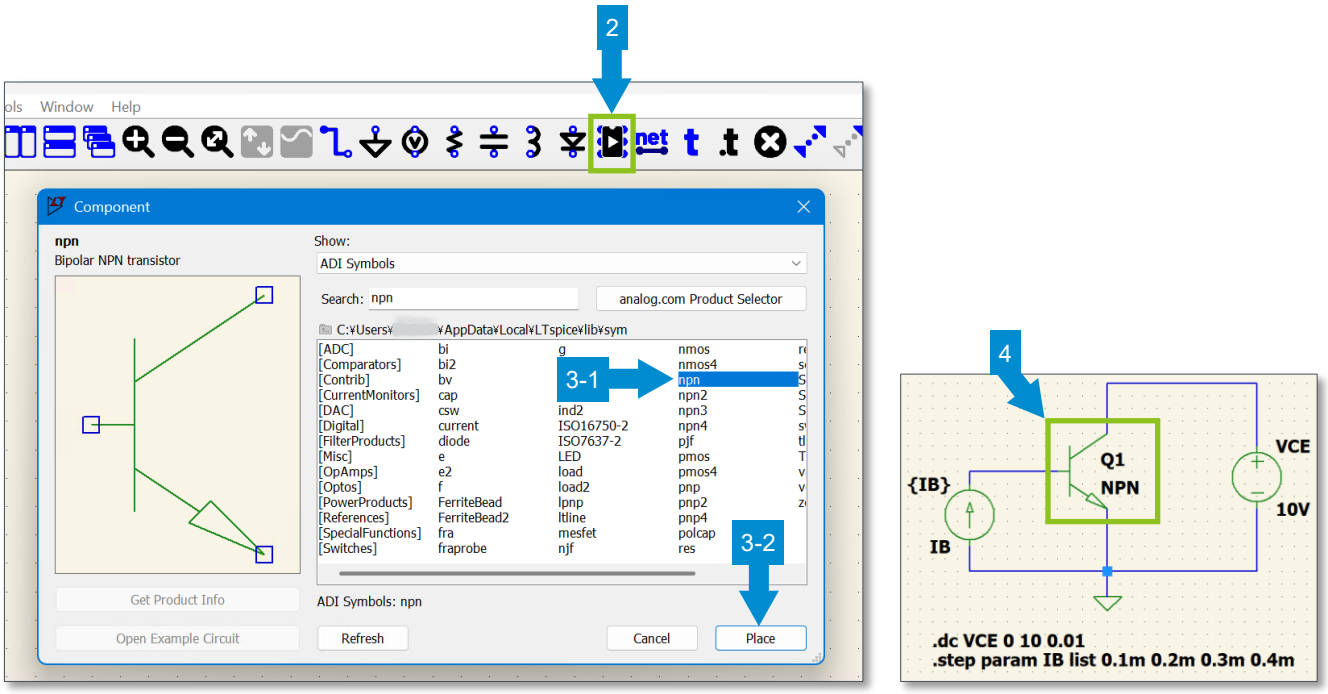
1. Store the model to be added in folder “`C:\Users\%USERNAME%\Documents\LTspice\lib\sub\MyLib`”.



2. Place the transistor on the circuit diagram. On the toolbar, click the “Component” icon to open “Component select window”.

3. From the list, select “npn” and then click “Place”. Select “pnp” for a PNP transistor, “diode” for a diode, and “LED” for an LED.

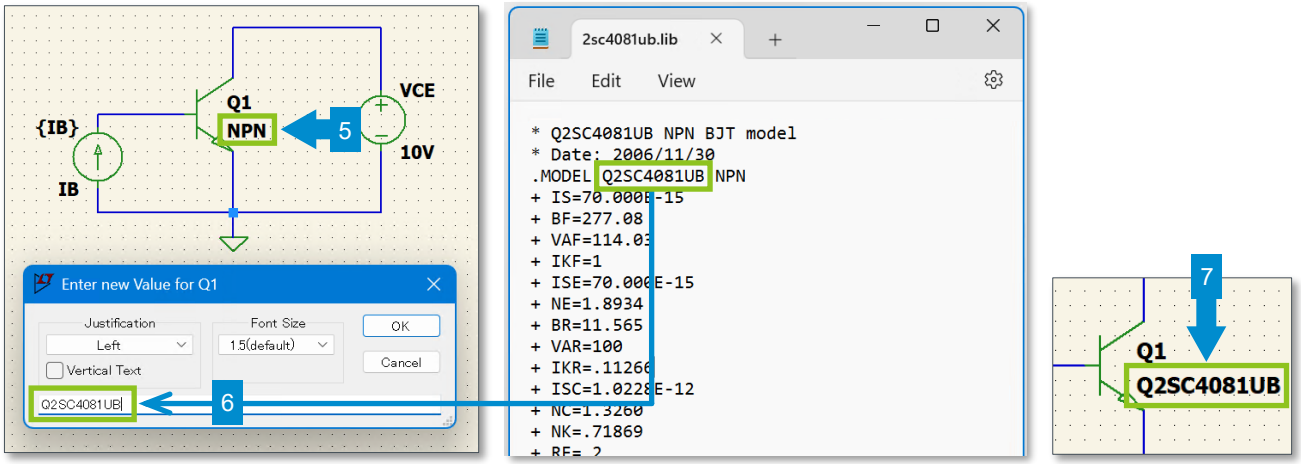
4. Place the component on the circuit diagram.



5. Right-click on “NPN” of the transistor.

6. When the input window is opened, rename “NPN” with the model name and then click “OK”. For the model name to be entered, open the “.lib” file and use the model name written on the “.MODEL” line.

7. The model name on the circuit diagram is changed.

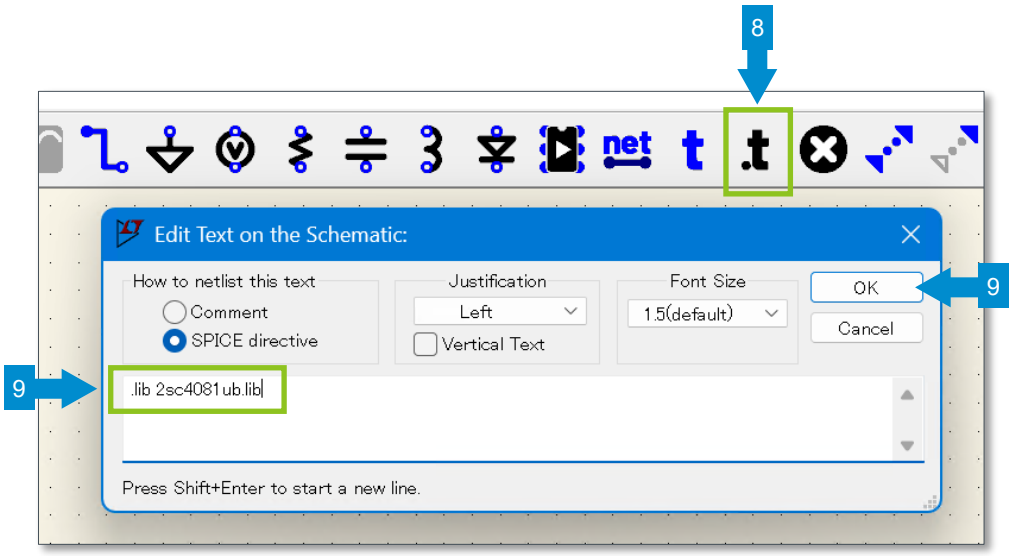


Next write the command to read the ".lib" file on the circuit diagram.

8. On the toolbar, click "Directive" to open the input window.
9. Enter "`.lib <filename>`" in the entry field. Note that `<filename>` should be the file name stored in the parts folder, but not the model name provided to the circuit symbol above. The format for describing `<filename>` depends on where the model is stored. Refer to the following for more details. After completing the input, click "OK".

   You can also use the "`.include`" and "`.inc`" commands in addition to "`.lib`".

Syntax	`.lib <filename>`
	`.include <filename>`
	`.inc <filename>`



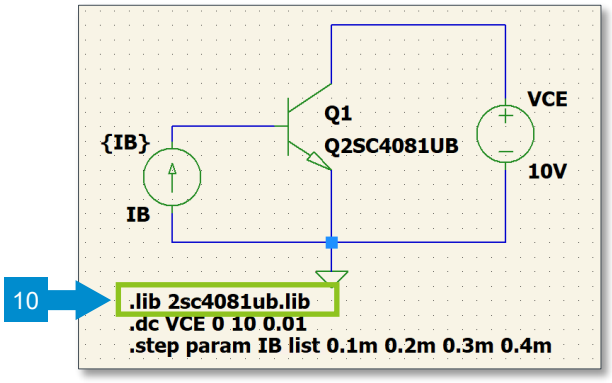
Description of `<filename>` depends on where the model is stored.

a. Same folder as the circuit diagram: `D:\project-a\test_circuit` ← example
   → Describe the file name only
   Syntax example: `.lib 2sc4081ub.lib`

b. Any folder: `C:\Users\%USERNAME%\Documents\LTspice\lib\sub\MyLib` ← example
   → Describe the absolute path and the file name
   Syntax example: `.lib C:\Users\%USERNAME%\Documents\LTspice\lib\sub\MyLib\2sc4081ub.lib`

For b above, you can also describe the file name only. In such cases, it is necessary to define the storage location of the device model files as described on the next page. This method is more convenient.

10. Place the command to read the "`.lib`" file at an appropriate location on the circuit diagram. This completes the setting.



The steps below must be performed if you describe only the file name in the "`.lib`" syntax in cases b on the previous page.

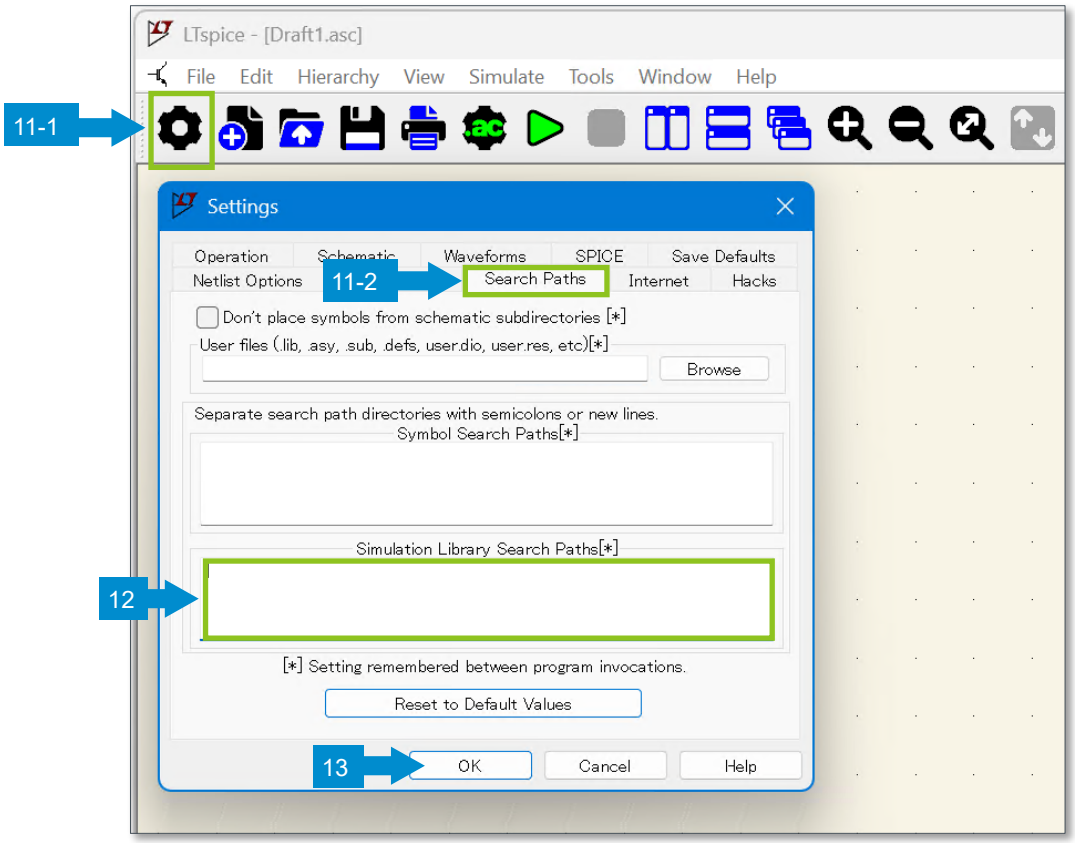
Define the storage location of the device model files. If the model storage location is changed, this method allows you to change the setting by batch on the Settings Dialog. Therefore, this method is more convenient compared with describing the absolute path of the model storage location in the "`.lib`" syntax.

11. On the toolbar, click the "Settings" icon. On the "Settings Dialog", open the "Search Paths" tab.

12. In the "Simulation Library Search Path[*]" field, describe the absolute path of the folder where the circuit model files are stored.

    Any folder: `C:\Users\%USERNAME%\Documents\LTspice\lib\sub\MyLib` ← example
    → Describe the absolute path
    Example of description: `C:\Users\%USERNAME%\Documents\LTspice\lib\sub\MyLib`

13. After completing the entry, click "OK". This completes the setting.



Subcircuit Models

6. Confirming the subcircuit models

For ROHM's products, the subcircuit models of MOSFET, SiC power devices, and IGBT are provided. Open the downloaded model file with a text editor and confirm that the syntax starts with ".SUBCKT".

7. How to add the subcircuit models

We explain two methods to add subcircuit models here. Since each method has advantages and disadvantages, select the method most suited for your application.

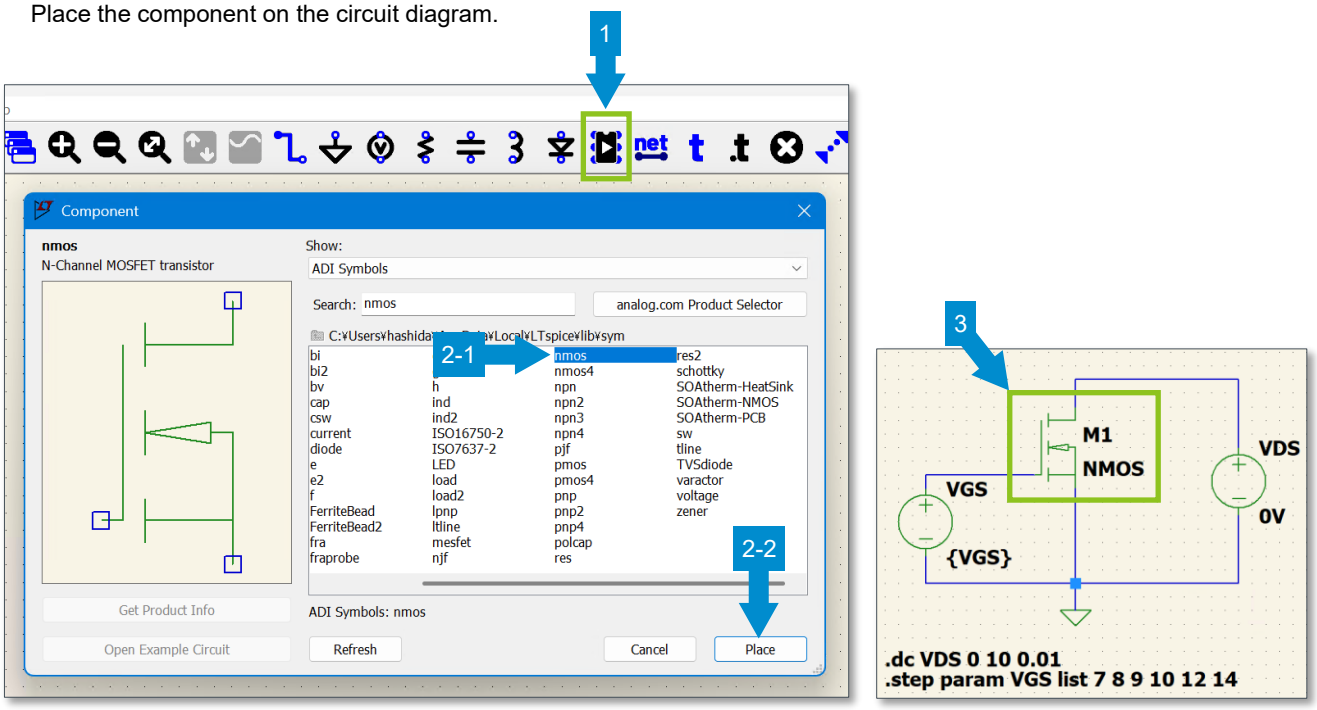
	Method 1 Describe the model information on the circuit diagram	Method 2 Store the model in a desired parts folder
Outline of the procedure	1. Place the symbol on the circuit diagram 2. Copy the model file to be added to "SPICE directive" in text format 3. Place the model text on the circuit diagram 4. Change the attributes of the symbol	1. Store the model file to be added in a folder 2. Create a circuit diagram symbol 3. Link the symbol and the model file 4. Define the storage location of the symbol and the model file 5. Place the symbol on the circuit diagram
Advantages	- Since the parameters of the parts are displayed on the circuit diagram, the simulation evidence can be checked with the circuit diagram only - Since simulations can be performed with the circuit diagram data only, they are independent of the PC environment	- Easy to manage the parts because they can be classified using folders
Disadvantages	- Many characters on the circuit diagram - Necessary to manage the parameters of the parts for each circuit diagram	- Requires tasks including creating the circuit diagram symbol and linking the symbol and the model file - Necessary to redo the environment setting of the symbols and the model files if the PC environment changes

In the following, we explain the procedure in more detail for each method.

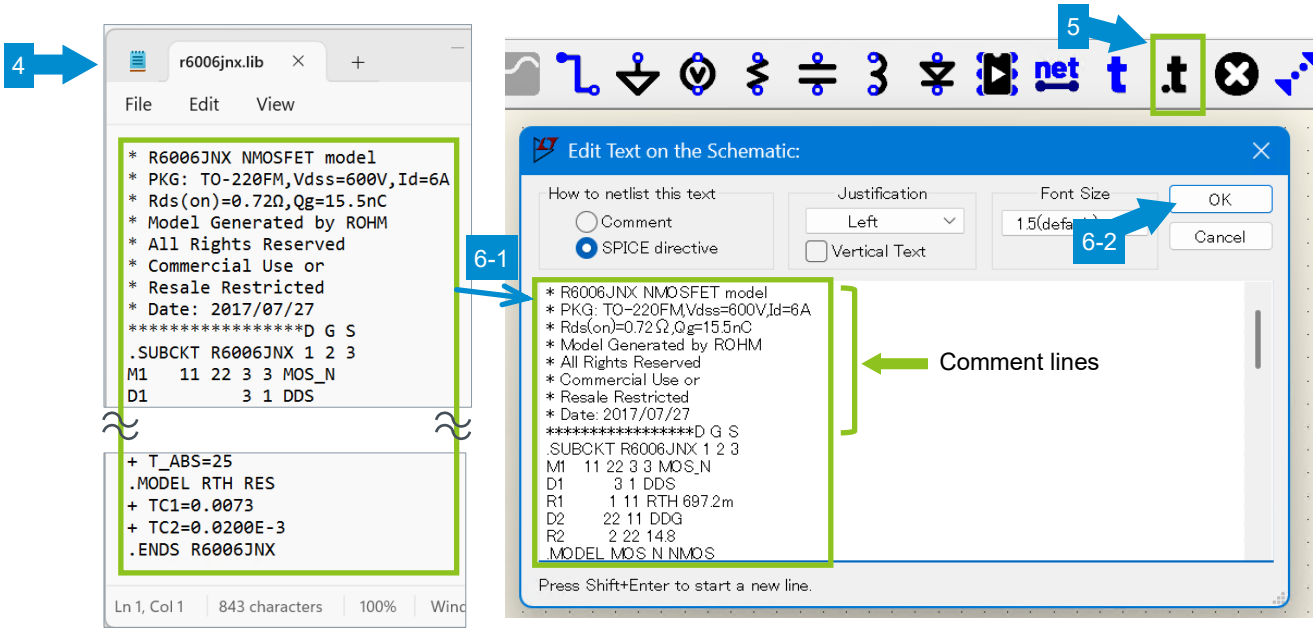
7-1. Method 1: Describe the model information on the circuit diagram

In this example, the Nch MOSFET “r6006jnx.lib” is added.

1. First, place the symbol on the circuit diagram. On the toolbar, click the “Component” icon to open “Component select window”.
2. From the list, select “nmos” and then click “Place”. For Pch MOSFET, select “pmos”. If the symbol you need is not listed, it must be created. We explain the method later.
3. Place the component on the circuit diagram.



4. Open the model to be added with a text editor (e.g. Notepad).
5. On the toolbar, click “SPICE Directive” to open the input window.
6. Copy the contents of the model and then click “OK”. At this time, you may delete unnecessary comment lines.

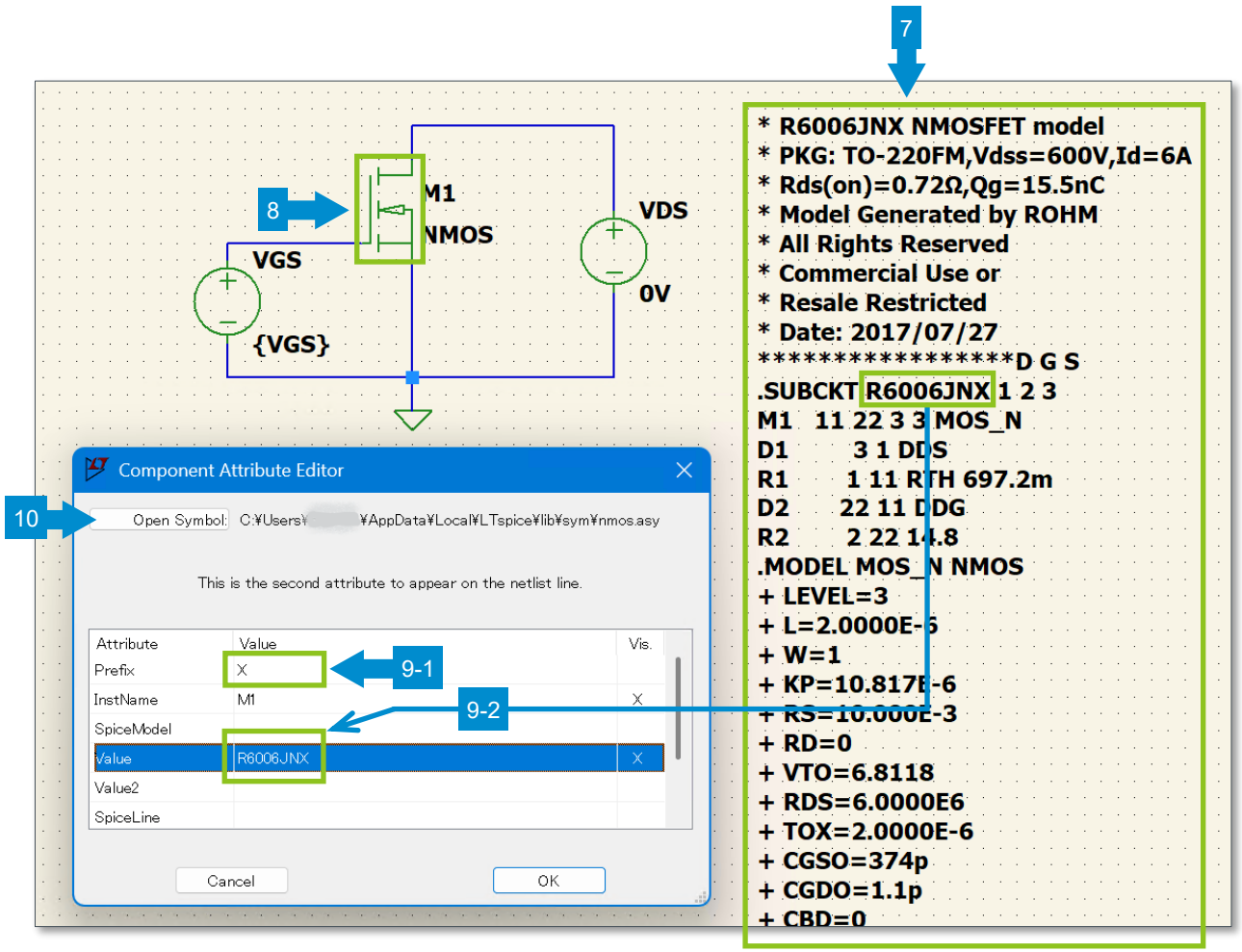


7. Place the model text at an appropriate location on the circuit diagram.

8. Ctrl + right-click on the circuit symbol.

9. When “Component Attribute Editor” is opened, change the attributes.
   - For the subcircuit models, update “Prefix” with “X”.
   - Update “Value” with the model name described in the “. SUBCKT” syntax of the subcircuit model file.

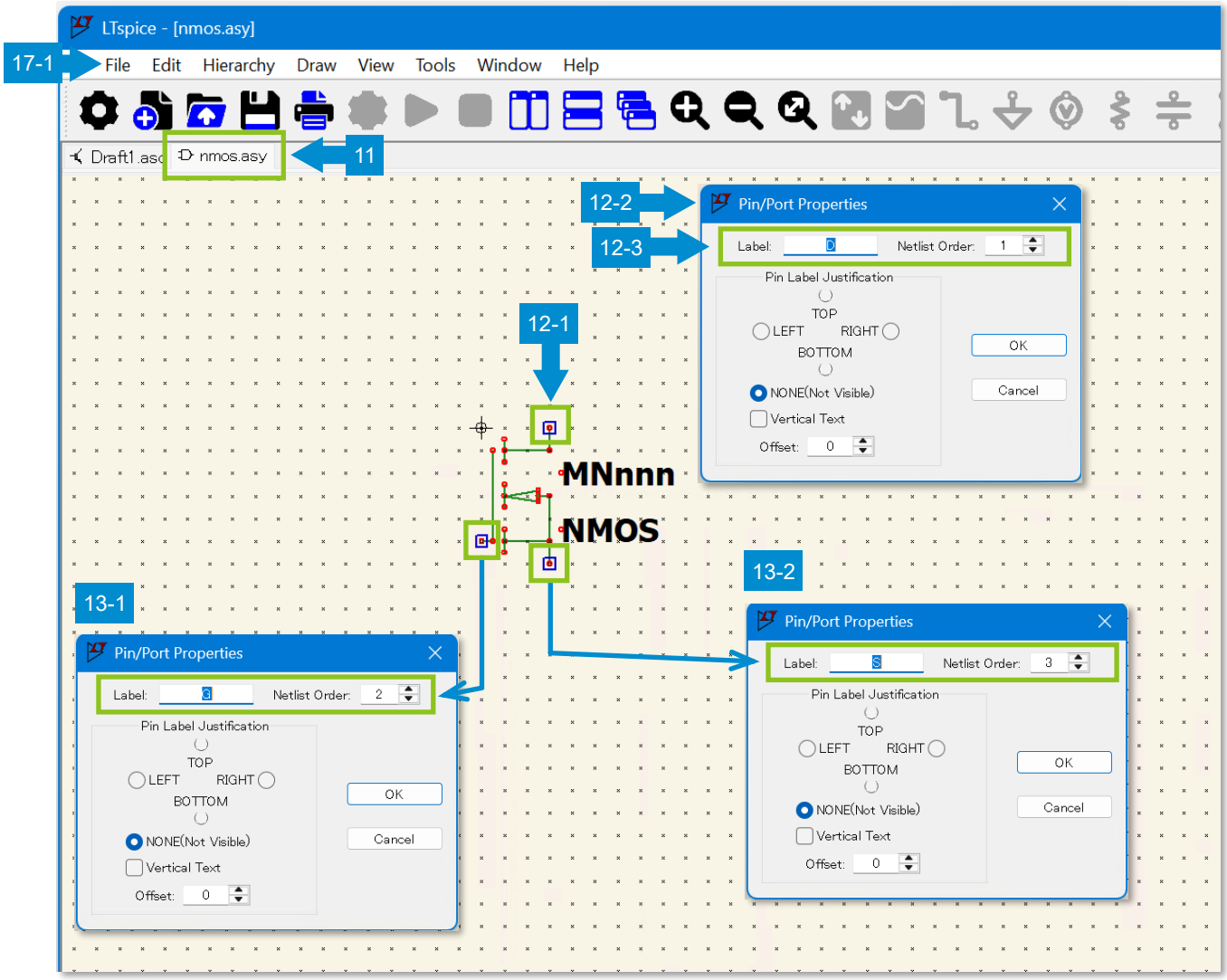
10. Click “Open Symbol” and check if the pin layout of the subcircuit model file (r6006jnx.lib) matches that of the circuit symbol (nmos.asy).



11. The Nch MOSFET symbol (nmos.asy) is displayed in a new tab.

12. Right-click on the symbol of the Drain pin to open the “Pin/Port Properties” window. Check “Label” and “Netlist Order”.

13. Check the Gate and Source pins in the same way. The results are shown below. It is confirmed that the pins are assigned 1, 2, and 3 in the order of D, G, and S.
    Label: D Netlist Order: 1
    Label: G Netlist Order: 2
    Label: S Netlist Order: 3

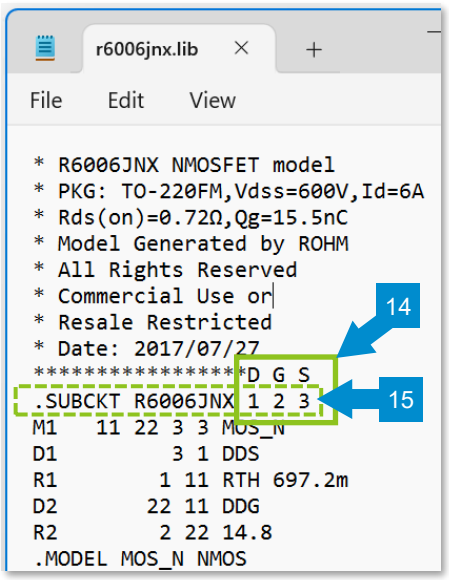


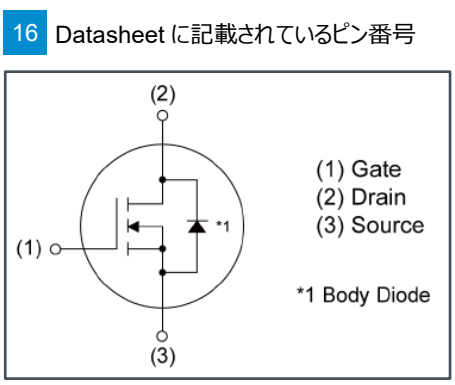
14. Check the order described in the subcircuit model file (r6006jnx.lib). The order is D, G, and S from the left. Therefore, the order is confirmed to be the same as the symbol setting.

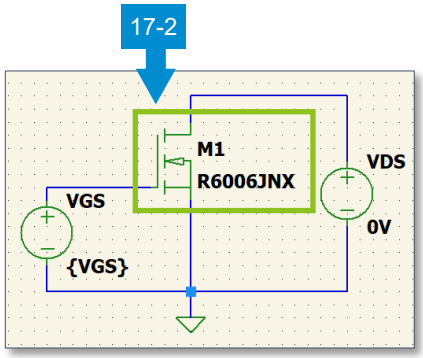
15. Note that “1 2 3” in the “.SUBCKT R6006JNX 1 2 3” syntax described in r6006jnx.lib is the node numbers of the subcircuit and not related to the numbers in “Netlist Order”.

16. It should also be noted that the numbers in “Netlist Order” are not the pin numbers described in the data sheet.

17. On the menu bar, click “File” and then “Close” to close the symbol. This completes the setting.







7-2. Method 2: Store the model in a desired parts folder

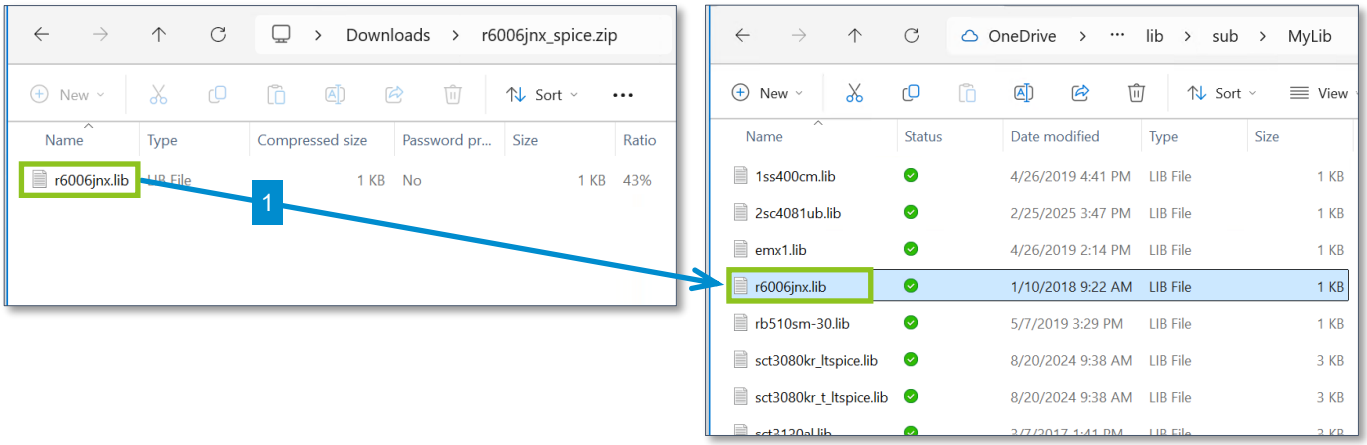
To distinguish the added models from the models installed as standard, you can create any folder and store the added models there. You can also store the added models in the same folder as the circuit diagram. In this way, you can store and use the models in a location where it is easy to manage them.

Examples of folders to store the models

a. Same folder as the circuit diagram : `D:\project-a\test_circuit` ← example
b. Any folder : `C:\Users\%USERNAME%\Documents\LTspice\lib\sub\MyLib` ← example
: `C:\Users\%USERNAME%\Documents\LTspice\lib\sub\ROHM` ←e.g., company name
: `E:\LTspicemodel\transistor\ROHM` ← example

As an example, we use a case where the Nch MOSFET model “r6006jnx.lib” is stored in an any folder.

1. Store the model to be added in the folder “`C:\Users\%USERNAME%\Documents\LTspice\lib\sub\Mylib`”.

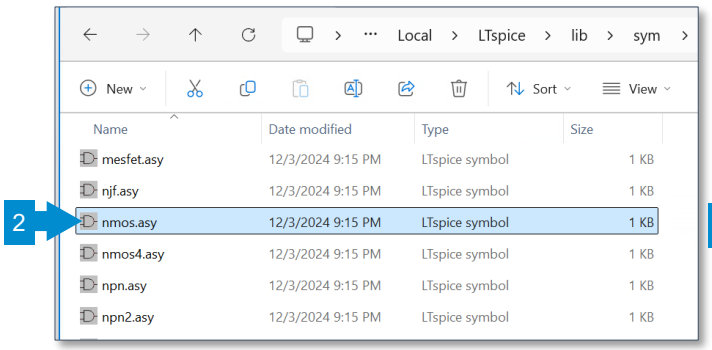


Create the circuit diagram symbol by using a circuit diagram symbol provided as standard

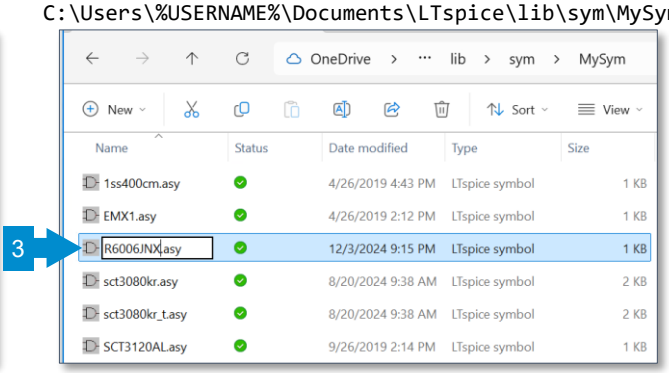
2. Copy “nmos.asy” in folder “C:\Users\%USERNAME%\AppData\Local\LTspice\lib\sym” to an any folder. If no standard symbol can be adapted, the symbol must be created using the method described below.

3. Change the name to “R6006JNX.asy”. In this example, the name is the same as the subcircuit model file name. However, this is not required and you can use any name recognizable to users.

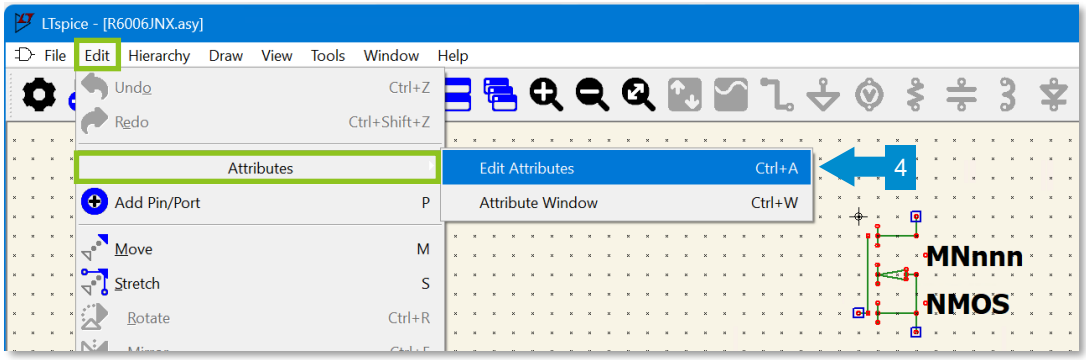
C:\Users\%USERNAME%\AppData\Local\LTspice\lib\sym



Copy to an any folder. e.g.
C:\Users\%USERNAME%\Documents\LTspice\lib\sym\MySym

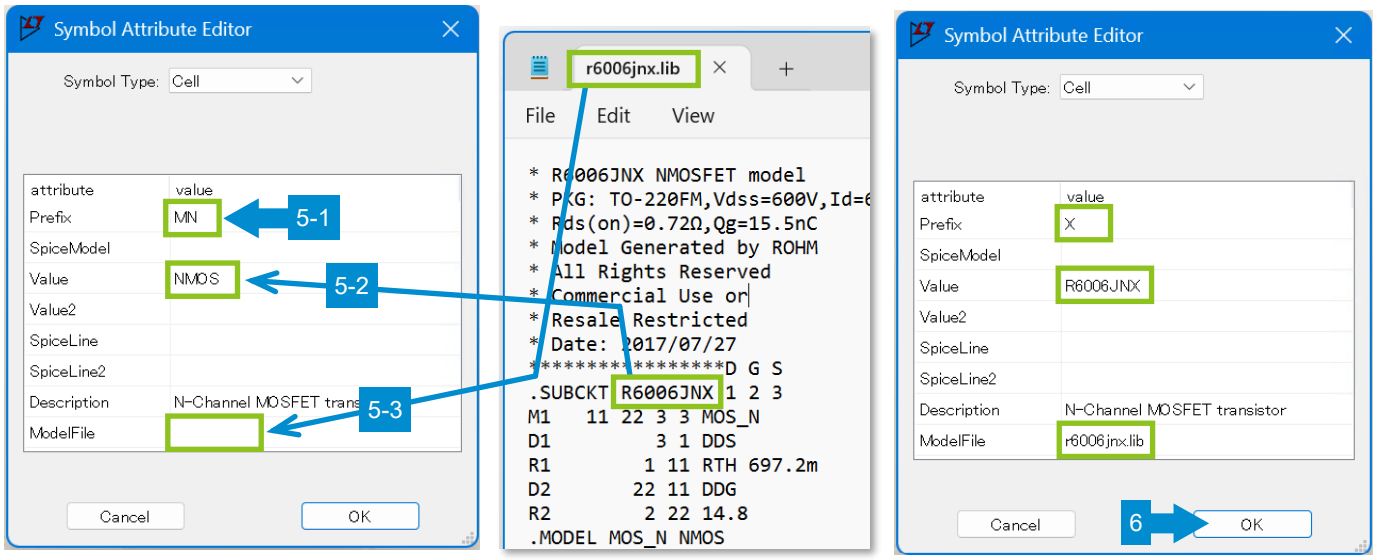


4. Open “R6006JNX.asy” with LTspice. On the menu bar, select “Edit” → “Attributes” → “Edit Attributes”.

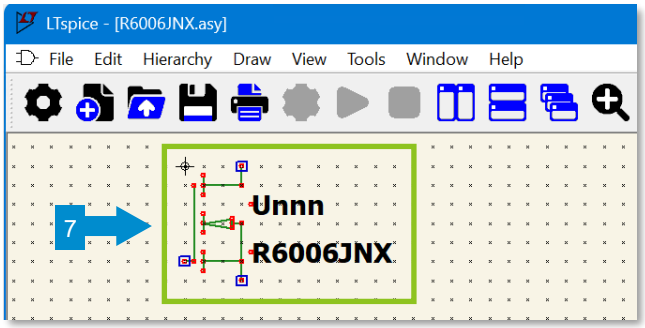


5. When “Symbol Attribute Editor” is opened, change the attributes.
   - For the subcircuit models, update “Prefix” with “X”.
   - Update “Value” with the model name described in the “. SUBCKT” syntax of the subcircuit model file.
   - Enter the subcircuit model file name in “ModelFile”.

6. Click “OK”.



7. The circuit symbol is now changed to “R6006JNX”.



Next, check if the pin layout of the subcircuit model file (r6006jnx.lib) matches that of the circuit symbol (R6006JNX.asy).

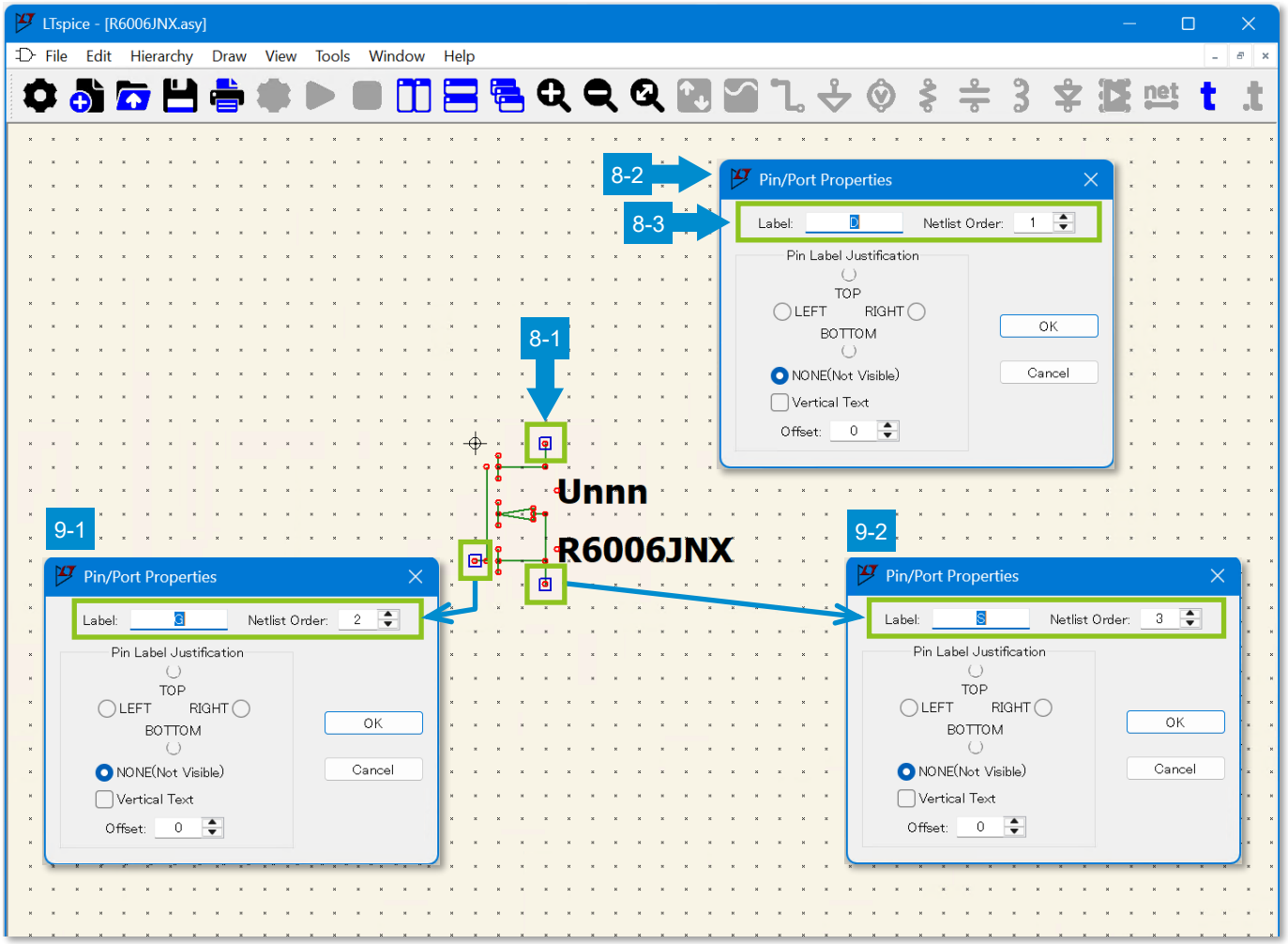
8. Right-click on the Drain pin symbol to open its property window. Check “Label” and “Netlist Order”.

9. Check the Gate and Source pins in the same way. The results are shown below. It is confirmed that the pins are assigned 1, 2, and 3 in the order of D, G, and S.

   Label: D Netlist Order: 1

   Label: G Netlist Order: 2

   Label: S Netlist Order: 3

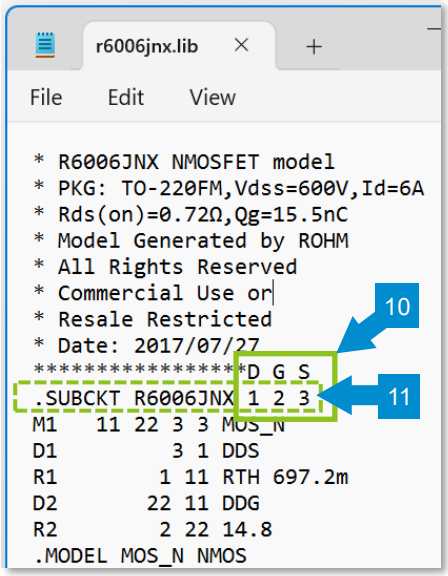


10. Check the order described in the subcircuit model file (r6006jnx.lib). The order is D, G, and S from the left. Therefore, the order is confirmed to be the same as the symbol setting. If they don't match, change the order of "Netlist Order".

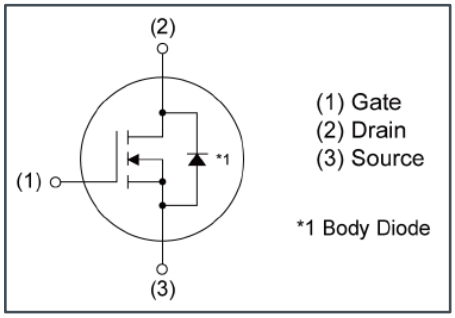
11. Note that "1 2 3" in the ".SUBCKT R6006JNX 1 2 3" syntax described in r6006jnx.lib is the node numbers of the subcircuit and not related to the numbers in "Netlist Order".

12. It should also be noted that the numbers in "Netlist Order" are not the pin numbers described in the data sheet.

13. On the menu bar, click "File" and then "Save" to save changes. Click "File" and then "Close" to close the symbol. This completes the setting.



12 Pin numbers described in the data sheet



Define the storage location of the symbol file.

The storage location must be defined if the symbol file is stored in a desired location like this example.

14. On the toolbar, click the “Settings” icon. On the “Settings Dialog”, open the “Search Paths” tab.

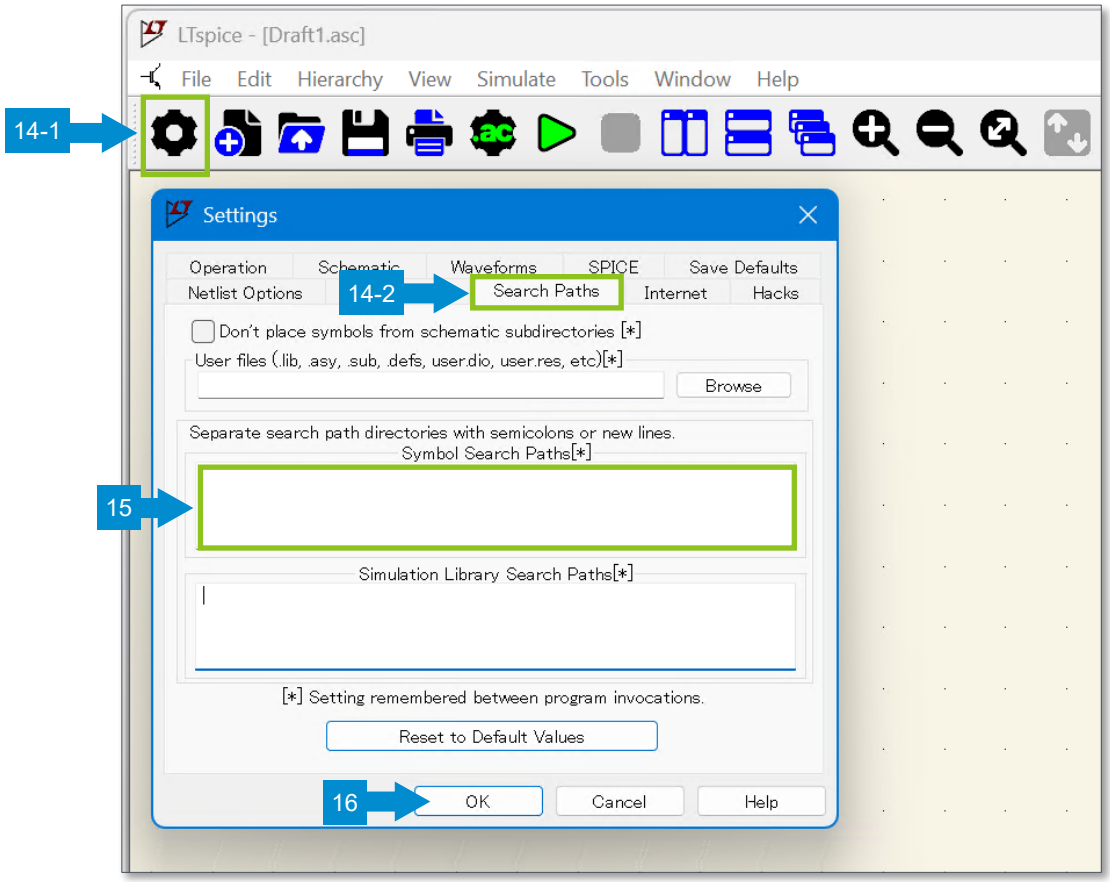
15. In the “Symbol Search Path[*]” field, describe the path of the folder where the circuit symbols are stored.

Any folder: `C:\Users\%USERNAME%\Documents\LTspice\lib\sym\MySym` ← example

→ Describe the absolute path

Example of description: `C:\Users\%USERNAME%\Documents\LTspice\lib\sym\MySym`

16. After completing the entry, click “OK”.



Define the storage location of the subcircuit model files.

The storage location must be defined if the subcircuit model file is stored in a desired location like this example.

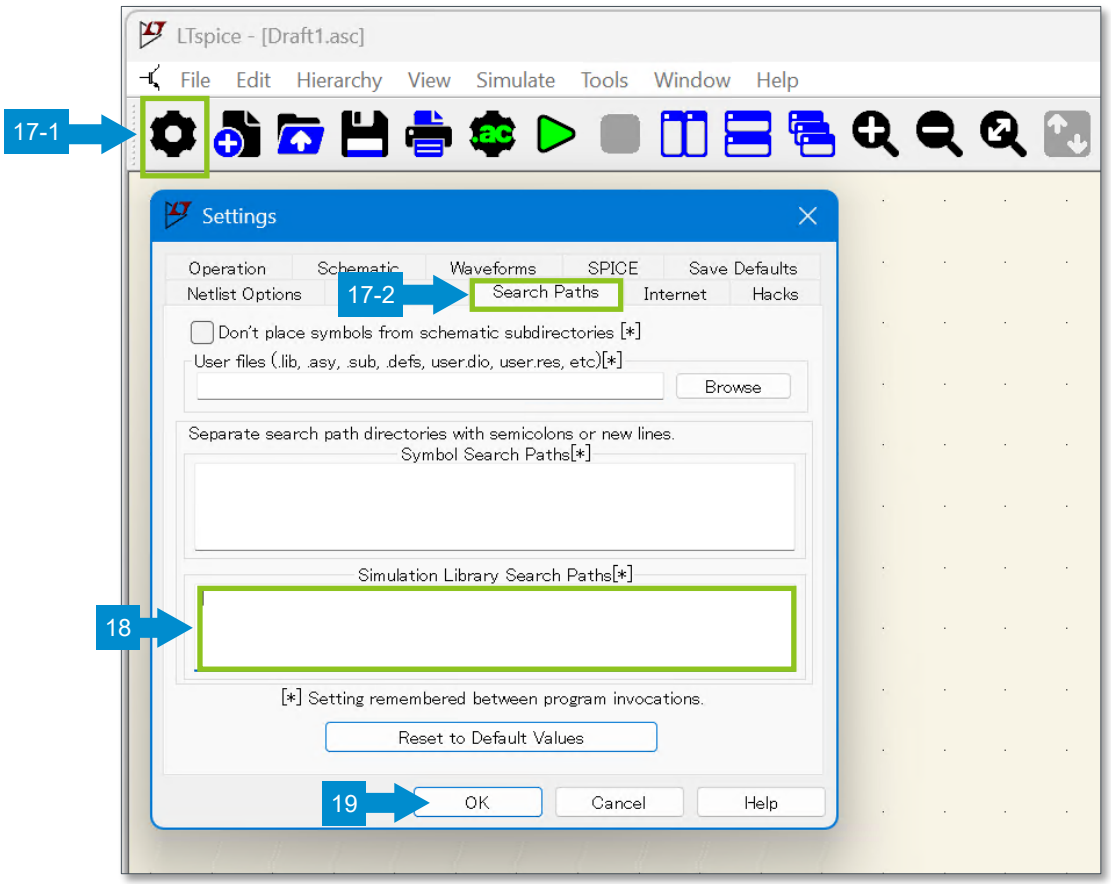
17. On the toolbar, click the “Settings” icon. On the “Settings Dialog”, open the “Search Paths” tab.

18. In the “Library Search Path[*]” field, describe the path of the folder where the circuit model files are stored. The format for describing the path depends on the storage location as follows.

    a. Same folder as the circuit diagram : `D:\project-a\test_circuit` ← example
    → No definition required

    b. Any folder : `C:\Users\%USERNAME%\Documents\LTspice\lib\sub\MyLib` ← example
    → Describe the absolute path
    Example of description: `C:\Users\%USERNAME%\Documents\LTspice\lib\sub\MyLib`

19. After completing the entry, click “OK”.



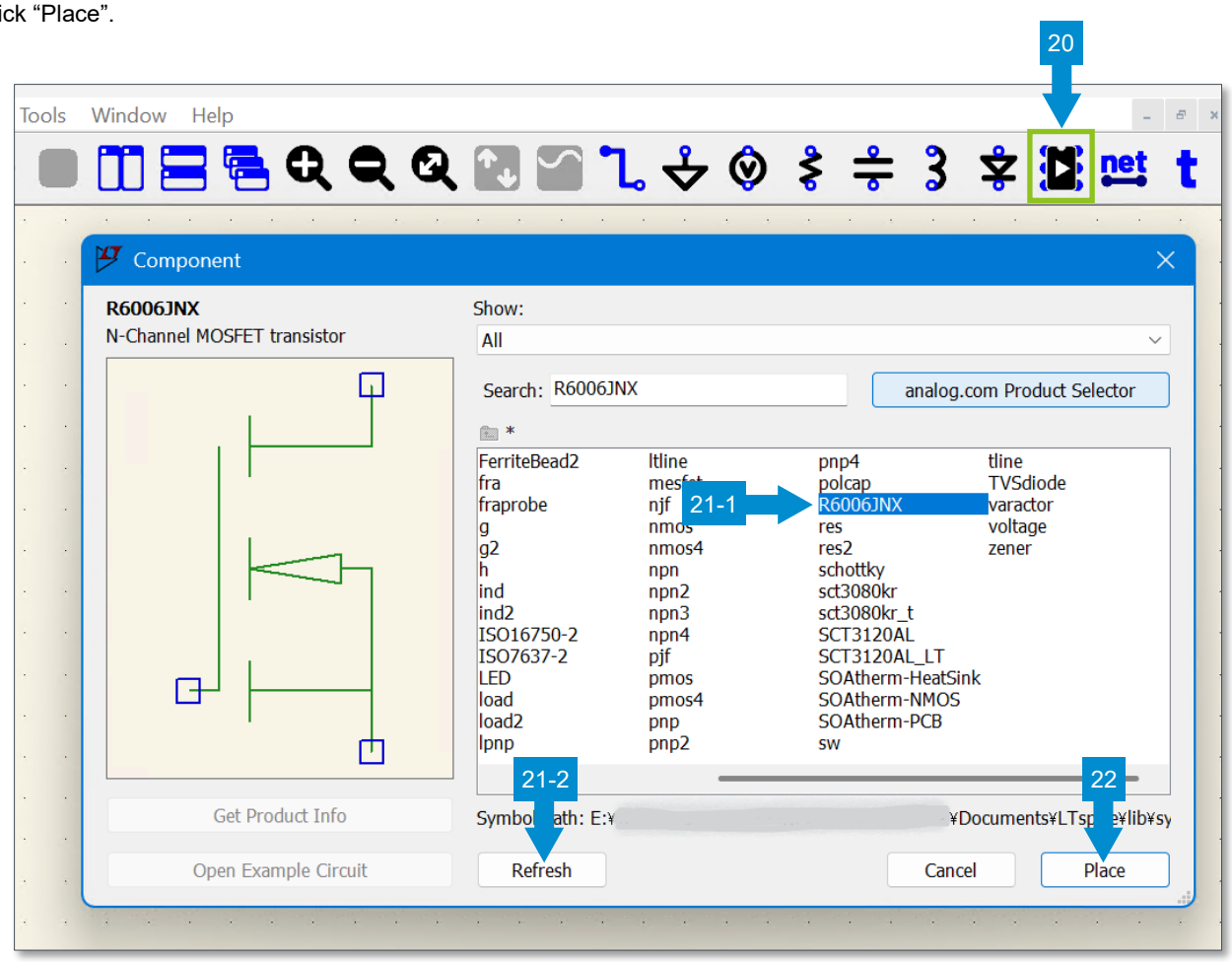
It is also possible to describe the path of the folder and place the symbol on the circuit diagram using the “`.lib`”, “`.include`”, and “`.inc`” syntaxes. However, if the model storage location is changed, the method described above is more convenient because it allows you to define the storage location on the “Settings Dialog” to change the settings by batch.

Place the circuit symbol on the circuit diagram.

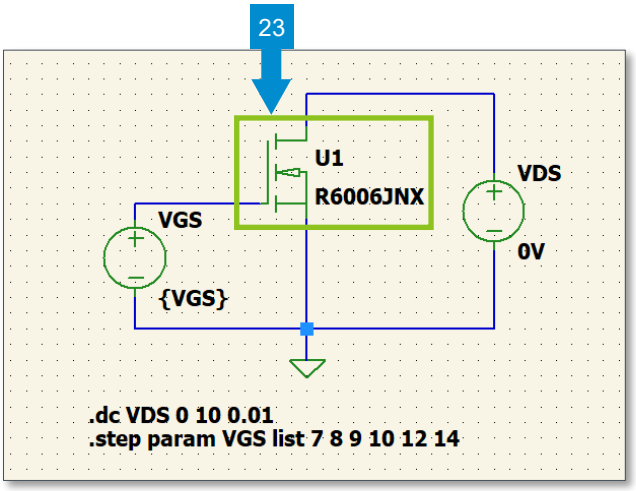
20. On the toolbar, click the “Component” icon to open “Component select window”.

21. From the list, select “R6006JNX” created above. The newly added symbol may not be displayed immediately. In such cases, click the “Refresh” button.

22. Click “Place”.



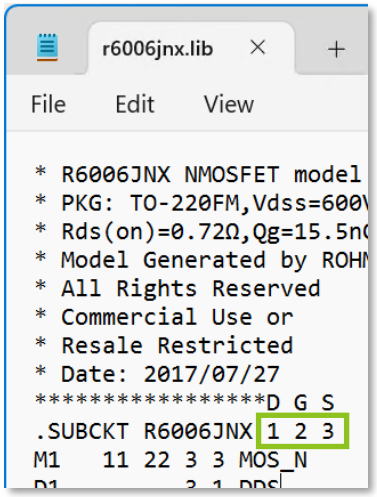
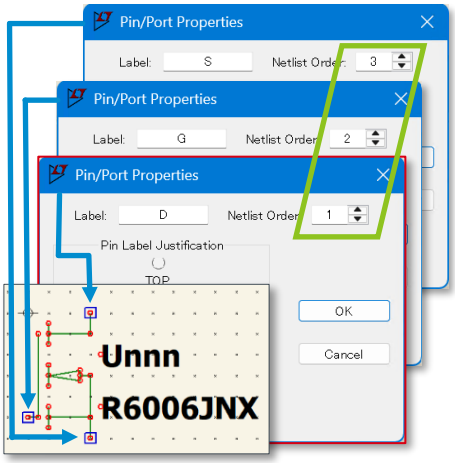
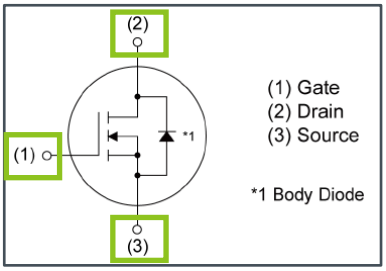
23. Place the component on the circuit diagram. This completes the setting.



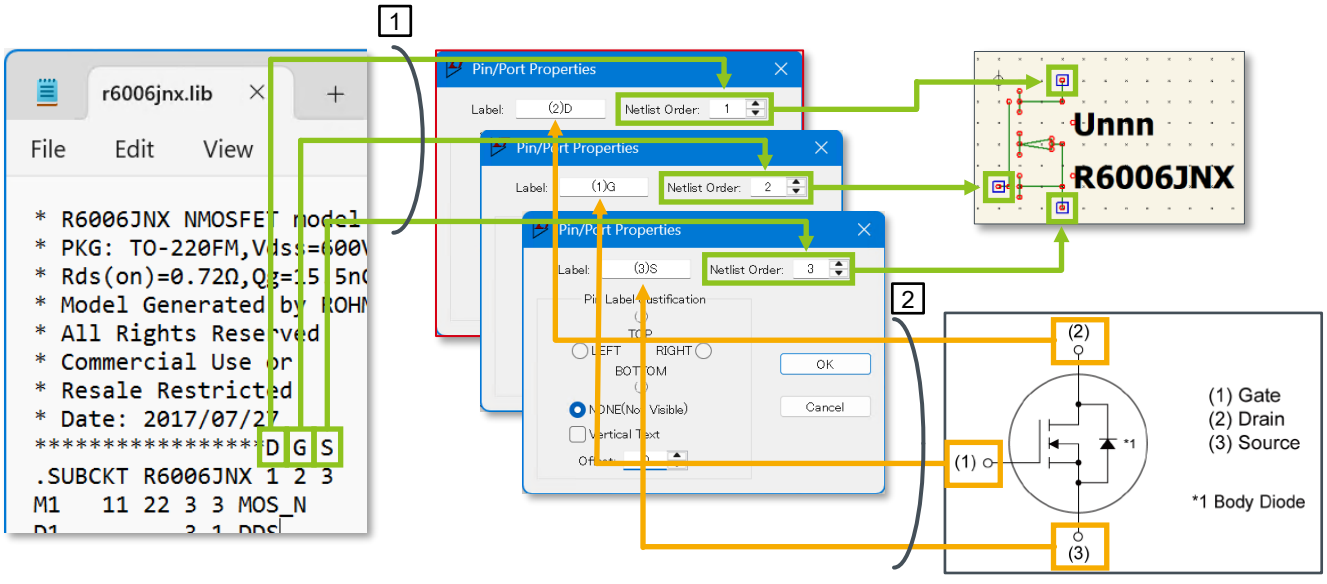
Supplementary: Precautions for matching the pin layouts of the subcircuit model file (.lib) and the circuit symbol (.asy)

For devices with a small number of pins, such as transistors, the net list and the property window of a circuit symbol show numbers “1”, “2”, and “3”. The internal circuit diagram in the data sheet also shows “1”, “2”, and “3”. Since these numbers have different meanings in these contexts, be careful not to consider them identical. Doing so will result in incorrect settings.

The table below summarizes the meaning of the numbers in each context. The numbers in the model file represent the node numbers of the subcircuit. They are different from the numbers in “Netlist Order” of the symbol or the pin numbers of the product. In this example, the node numbers are 1, 2, and 3 for D, G, and S, respectively, by chance. This causes a more confusing situation where the node numbers may be mistaken for the pin numbers. The numbers in “Netlist Order” of the circuit symbol represent the order of the pins described on the net list. In this example, “1” indicates that “D” is the leftmost pin on the net list. Similarly, “2” indicates that “G” is the second pin from left on the net list, and “3” indicates that “S” is the third pin from left on the net list. The numbers shown on the internal circuit diagram in the data sheet are the pin numbers of the product. These numbers are used for the physical pin layout.

Model file (net list)	Circuit symbol	Internal circuit diagram in the data sheet
Node numbers of the subcircuit	Order of the pins described in the net list	Pin numbers of the product
		

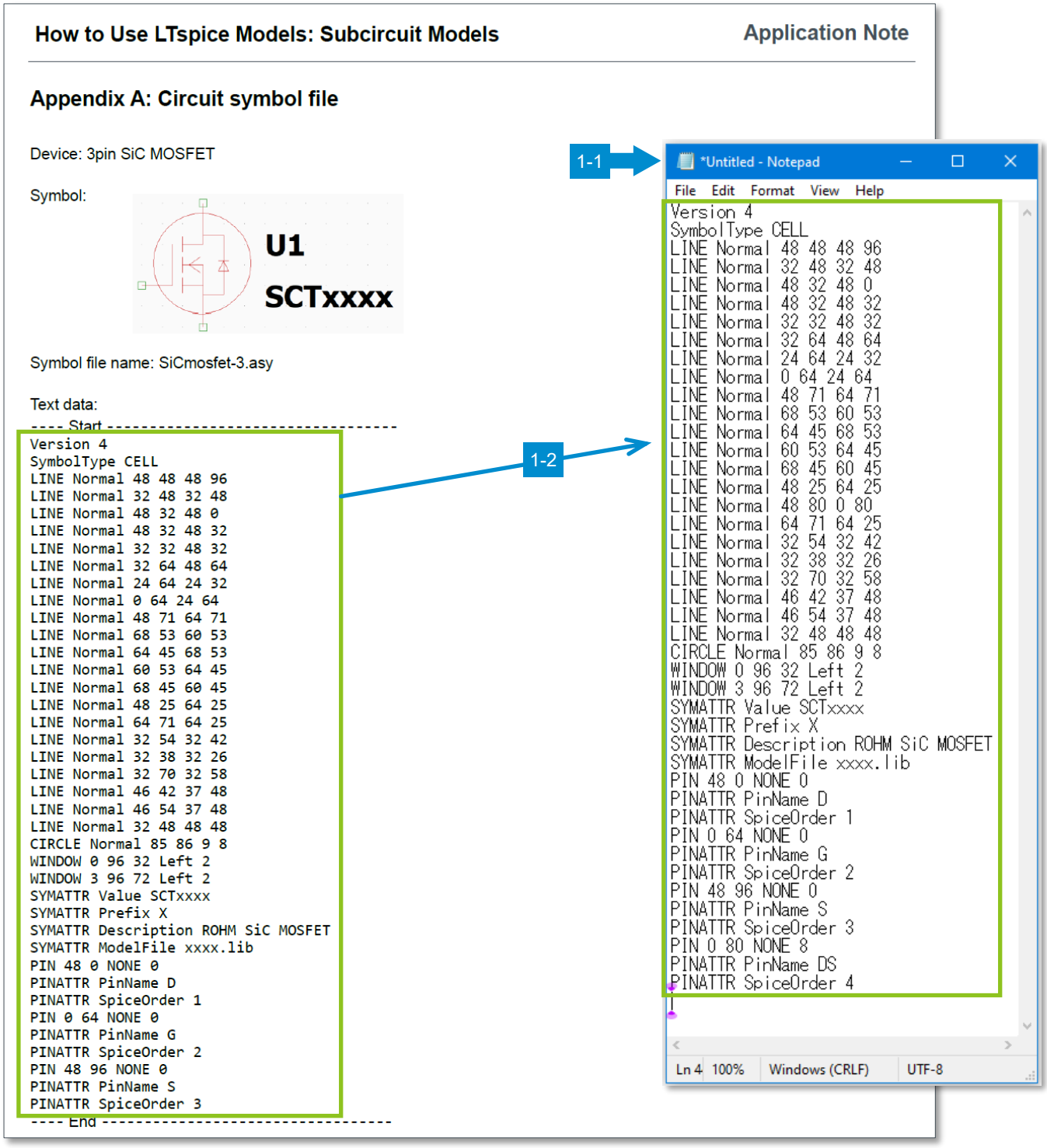
The figure below summarizes the details for matching the pin layouts. 1. Match the order of the pins described in the subcircuit model file with the order in “Netlist Order” of the circuit diagram symbol. 2. To display the physical pin layout shown in the data sheet as the symbol information, define it in the “Label” field.



8. How to create circuit diagram symbols

You can create symbols that are not provided as standard, such as SiC MOSFET and IGBT. Although it is possible to create a symbol from scratch using the “Draw” tool, it takes a long time with this method. Therefore, we explain how to create a symbol from a provided symbol file (.asy). The circuit symbol files are shown as appendices to this application note. Select the required symbol from the appendices to create your symbol.

1. Open a new file with a text editor (Notepad). Copy and paste the text data section of the symbol to be created from the appendices to the new file.

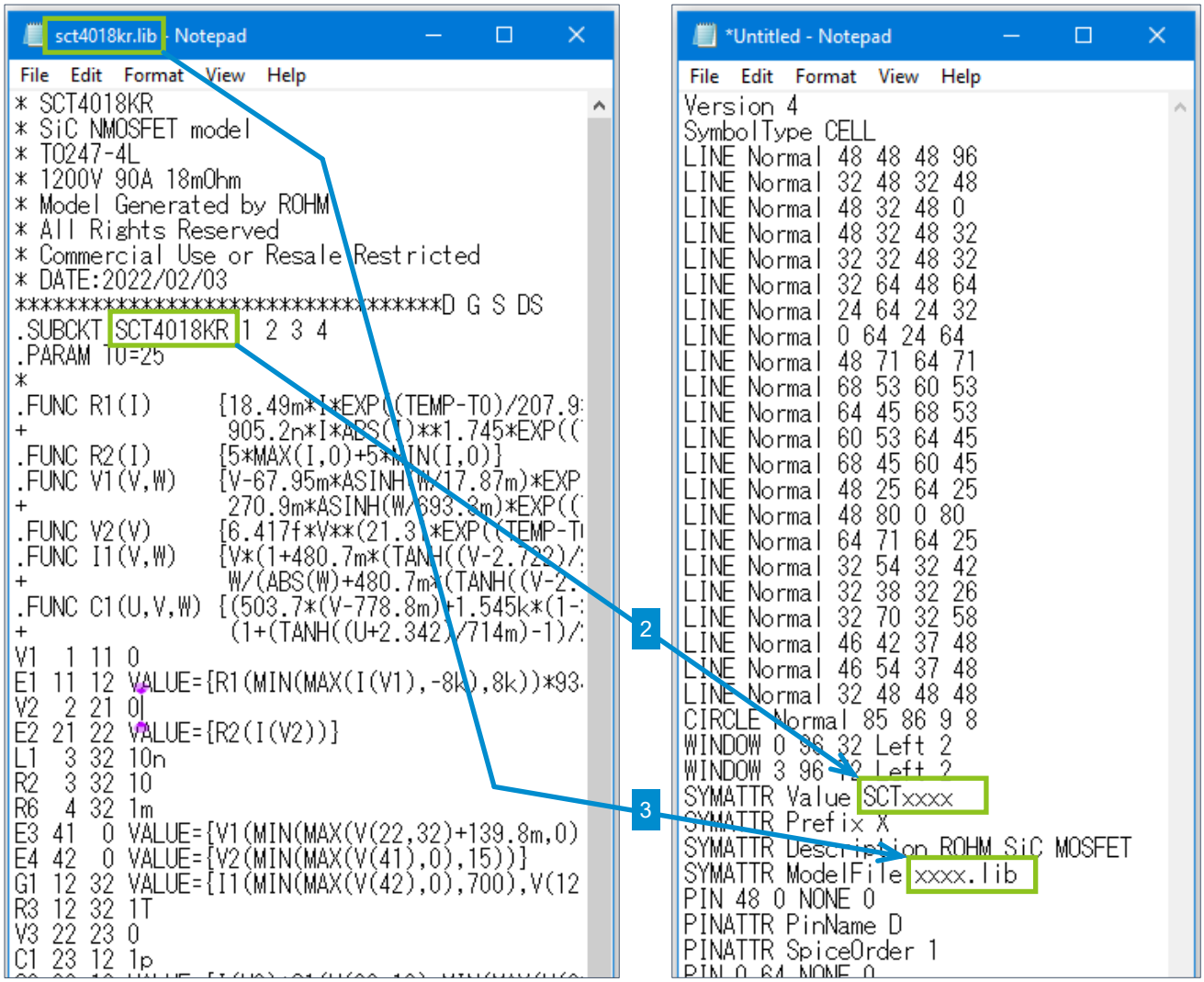


2. Open the subcircuit model corresponding to the symbol with a text editor. Enter the model name described in the ".SUBCKT" syntax for the value of the "SYMATTR Value" syntax in the symbol file being created.

3. Enter the file name of the subcircuit model for the value of the "SYMATTR ModelFile" syntax in the symbol file being created.

Subcircuit model file (.lib)

Symbol file being created (.asy)

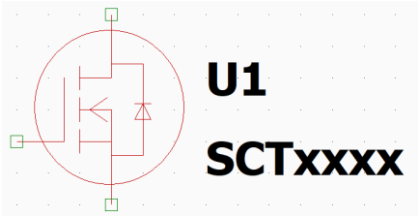


4. Save the symbol file with an appropriate file name and extension ".asy" (e.g. SCT4018KR.asy). This completes the creation of the symbol.

Appendix 1 : Circuit symbol file

“SiC MOSFET 3-pin”

Symbol:



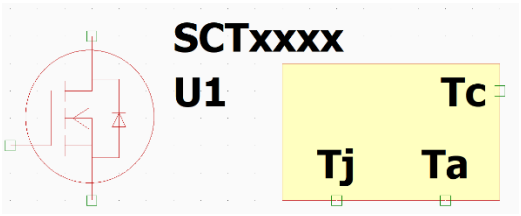
Symbol file name: SiCmosfet-3.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 48 48 48 96
LINE Normal 32 48 32 48
LINE Normal 48 32 48 0
LINE Normal 48 32 48 32
LINE Normal 32 32 48 32
LINE Normal 32 64 48 64
LINE Normal 24 64 24 32
LINE Normal 0 64 24 64
LINE Normal 48 71 64 71
LINE Normal 68 53 60 53
LINE Normal 64 45 68 53
LINE Normal 60 53 64 45
LINE Normal 68 45 60 45
LINE Normal 48 25 64 25
LINE Normal 64 71 64 25
LINE Normal 32 54 32 42
LINE Normal 32 38 32 26
LINE Normal 32 70 32 58
LINE Normal 46 42 37 48
LINE Normal 46 54 37 48
LINE Normal 32 48 48 48
CIRCLE Normal 85 86 9 8
WINDOW 0 96 32 Left 2
WINDOW 3 96 72 Left 2
SYMATTR Value SCTxxxx
SYMATTR Prefix X
SYMATTR Description ROHM SiC MOSFET
SYMATTR ModelFile xxxx.lib
PIN 48 0 NONE 0
PINATTR PinName D
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName G
PINATTR SpiceOrder 2
PIN 48 96 NONE 0
PINATTR PinName S
PINATTR SpiceOrder 3
---- End ----------------------------------
```

Appendix 2 : Circuit symbol file
“SiC MOSFET 3-pin (coupled electro-thermal analysis model)”

Symbol:



Symbol file name: SiCmosfet-3-therm.asy

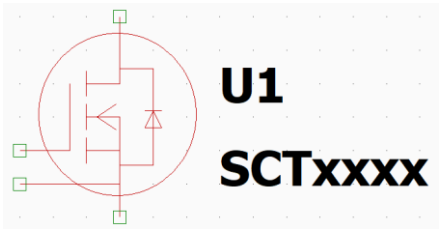
Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 48 48 48 96
LINE Normal 32 48 32 48
LINE Normal 48 32 48 0
LINE Normal 48 32 48 32
LINE Normal 32 32 48 32
LINE Normal 32 64 48 64
LINE Normal 24 64 24 32
LINE Normal 0 64 24 64
LINE Normal 48 71 64 71
LINE Normal 68 53 60 53
LINE Normal 64 45 68 53
LINE Normal 60 53 64 45
LINE Normal 68 45 60 45
LINE Normal 48 25 64 25
LINE Normal 64 71 64 25
LINE Normal 32 54 32 42
LINE Normal 32 38 32 26
LINE Normal 32 70 32 58
LINE Normal 46 42 37 48
LINE Normal 46 54 37 48
LINE Normal 32 48 48 48
RECTANGLE Normal 288 96 160 16
CIRCLE Normal 85 86 9 8
WINDOW 0 96 32 Left 2
WINDOW 3 96 0 Left 2
SYMATTR Value SCTxxxx
SYMATTR Prefix X
SYMATTR Description ROHM SiC MOSFET
SYMATTR ModelFile xxxx.lib
PIN 48 0 NONE 0
PINATTR PinName D
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName G
PINATTR SpiceOrder 2
PIN 48 96 NONE 0
PINATTR PinName S
PINATTR SpiceOrder 3
PIN 192 96 BOTTOM 8
PINATTR PinName Tj
PINATTR SpiceOrder 4
PIN 256 96 BOTTOM 8
PINATTR PinName Ta
PINATTR SpiceOrder 6
PIN 288 32 RIGHT 8
PINATTR PinName Tc
PINATTR SpiceOrder 5
---- End ----------------------------------
```

Appendix 3 : Circuit symbol file

“SiC MOSFET 4-pin”

Symbol:



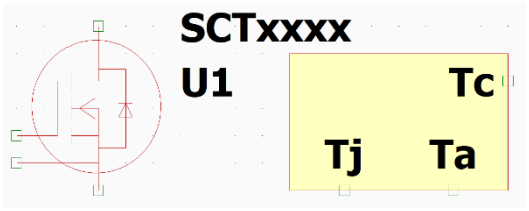
Symbol file name: SiCmosfet-4.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 48 48 48 96
LINE Normal 32 48 32 48
LINE Normal 48 32 48 0
LINE Normal 48 32 48 32
LINE Normal 32 32 48 32
LINE Normal 32 64 48 64
LINE Normal 24 64 24 32
LINE Normal 0 64 24 64
LINE Normal 48 71 64 71
LINE Normal 68 53 60 53
LINE Normal 64 45 68 53
LINE Normal 60 53 64 45
LINE Normal 68 45 60 45
LINE Normal 48 25 64 25
LINE Normal 48 80 0 80
LINE Normal 64 71 64 25
LINE Normal 32 54 32 42
LINE Normal 32 38 32 26
LINE Normal 32 70 32 58
LINE Normal 46 42 37 48
LINE Normal 46 54 37 48
LINE Normal 32 48 48 48
CIRCLE Normal 85 86 9 8
WINDOW 0 96 32 Left 2
WINDOW 3 96 72 Left 2
SYMATTR Value SCTxxxx
SYMATTR Prefix X
SYMATTR Description ROHM SiC MOSFET
SYMATTR ModelFile xxxx.lib
PIN 48 0 NONE 0
PINATTR PinName D
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName G
PINATTR SpiceOrder 2
PIN 48 96 NONE 0
PINATTR PinName S
PINATTR SpiceOrder 3
PIN 0 80 NONE 8
PINATTR PinName DS
PINATTR SpiceOrder 4
---- End ------------------------------------
```

Appendix 4 : Circuit symbol file
“SiC MOSFET 4-pin (coupled electro-thermal analysis model)”

Symbol:



Symbol file name: SiCmosfet-4-therm.asy

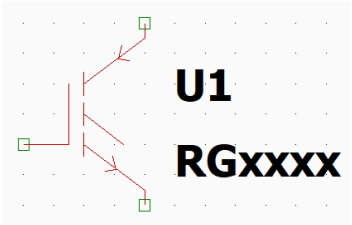
Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 48 48 48 96
LINE Normal 32 48 32 48
LINE Normal 48 32 48 0
LINE Normal 48 32 48 32
LINE Normal 32 32 48 32
LINE Normal 32 64 48 64
LINE Normal 24 64 24 32
LINE Normal 0 64 24 64
LINE Normal 48 71 64 71
LINE Normal 68 53 60 53
LINE Normal 64 45 68 53
LINE Normal 60 53 64 45
LINE Normal 68 45 60 45
LINE Normal 48 25 64 25
LINE Normal 48 80 0 80
LINE Normal 64 71 64 25
LINE Normal 32 54 32 42
LINE Normal 32 38 32 26
LINE Normal 32 70 32 58
LINE Normal 46 42 37 48
LINE Normal 46 54 37 48
LINE Normal 32 48 48 48
RECTANGLE Normal 288 96 160 16
CIRCLE Normal 85 86 9 8
WINDOW 0 96 32 Left 2
WINDOW 3 96 0 Left 2
SYMATTR Value SCTxxxx
SYMATTR Prefix X
SYMATTR Description ROHM SiC MOSFET
SYMATTR ModelFile xxxx.lib
PIN 48 0 NONE 0
PINATTR PinName D
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName G
PINATTR SpiceOrder 2
PIN 48 96 NONE 0
PINATTR PinName S
PINATTR SpiceOrder 3
PIN 0 80 NONE 8
PINATTR PinName DS
PINATTR SpiceOrder 4
PIN 192 96 BOTTOM 8
PINATTR PinName Tj
PINATTR SpiceOrder 5
PIN 288 32 RIGHT 8
PINATTR PinName Tc
PINATTR SpiceOrder 6
PIN 256 96 BOTTOM 8
PINATTR PinName Ta
PINATTR SpiceOrder 7
---- End ----------------------------------
```

Appendix 5 : Circuit symbol file

“IGBT”

Symbol:



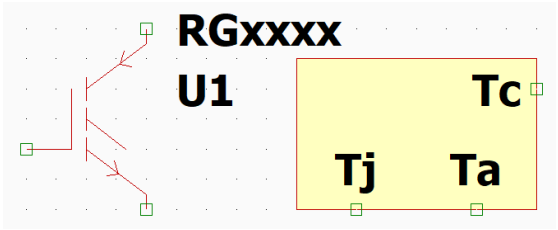
Symbol file name: IGBT.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 64 8 64 0
LINE Normal 64 8 64 8
LINE Normal 24 64 24 32
LINE Normal 0 64 24 64
LINE Normal 64 96 64 88
LINE Normal 32 54 32 42
LINE Normal 32 38 32 26
LINE Normal 32 70 32 58
LINE Normal 64 8 32 32
LINE Normal 64 88 32 64
LINE Normal 53 64 32 48
LINE Normal 47 70 49 77
LINE Normal 43 78 49 77
LINE Normal 56 20 50 19
LINE Normal 52 12 50 19
WINDOW 0 80 32 Left 2
WINDOW 3 80 72 Left 2
SYMATTR Value RGxxxx
SYMATTR Prefix X
SYMATTR Description ROHM IGBT
SYMATTR ModelFile xxxx.lib
PIN 64 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName G
PINATTR SpiceOrder 2
PIN 64 96 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
---- End ----------------------------------
```

Appendix 6 : Circuit symbol file
“IGBT (coupled electro-thermal analysis model)”

Symbol:



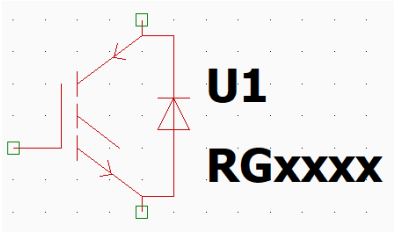
Symbol file name: IGBT-therm.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 64 8 64 0
LINE Normal 64 8 64 8
LINE Normal 24 64 24 32
LINE Normal 0 64 24 64
LINE Normal 64 96 64 88
LINE Normal 32 54 32 42
LINE Normal 32 38 32 26
LINE Normal 32 70 32 58
LINE Normal 64 8 32 32
LINE Normal 64 88 32 64
LINE Normal 53 64 32 48
LINE Normal 47 70 49 77
LINE Normal 43 78 49 77
LINE Normal 56 20 50 19
LINE Normal 52 12 50 19
RECTANGLE Normal 272 96 144 16
WINDOW 0 80 32 Left 2
WINDOW 3 80 0 Left 2
SYMATTR Value RGxxxx
SYMATTR Prefix X
SYMATTR Description ROHM IGBT
SYMATTR ModelFile xxxx.lib
PIN 64 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName G
PINATTR SpiceOrder 2
PIN 64 96 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
PIN 176 96 BOTTOM 8
PINATTR PinName Tj
PINATTR SpiceOrder 4
PIN 272 32 RIGHT 8
PINATTR PinName Tc
PINATTR SpiceOrder 5
PIN 240 96 BOTTOM 8
PINATTR PinName Ta
PINATTR SpiceOrder 6
---- End ------------------------------------
```

Appendix 7 : Circuit symbol file
“IGBT with built-in fast recovery diode”

Symbol:



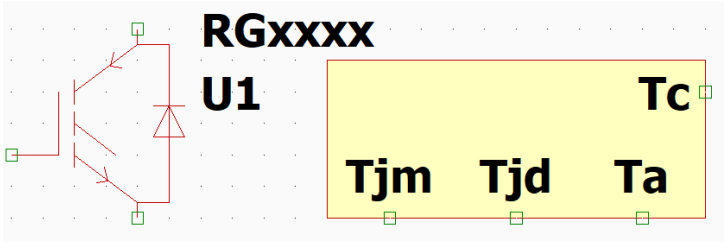
Symbol file name: IGBT-frd.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 64 8 64 0
LINE Normal 64 8 64 8
LINE Normal 24 64 24 32
LINE Normal 0 64 24 64
LINE Normal 80 88 80 8
LINE Normal 64 8 80 8
LINE Normal 64 96 64 88
LINE Normal 64 88 80 88
LINE Normal 88 55 72 55
LINE Normal 80 39 88 55
LINE Normal 72 55 80 39
LINE Normal 88 39 72 39
LINE Normal 32 54 32 42
LINE Normal 32 38 32 26
LINE Normal 32 70 32 58
LINE Normal 64 8 32 32
LINE Normal 64 88 32 64
LINE Normal 53 64 32 48
LINE Normal 47 70 49 77
LINE Normal 43 78 49 77
LINE Normal 56 20 50 19
LINE Normal 52 12 50 19
WINDOW 0 96 32 Left 2
WINDOW 3 96 72 Left 2
SYMATTR Value RGxxxx
SYMATTR Prefix X
SYMATTR Description ROHM IGBT
SYMATTR ModelFile xxxx.lib
PIN 64 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName G
PINATTR SpiceOrder 2
PIN 64 96 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
---- End ------------------------------------
```

Appendix 8 : Circuit symbol file
“IGBT with built-in fast recovery diode (coupled electro-thermal analysis model)”

Symbol:



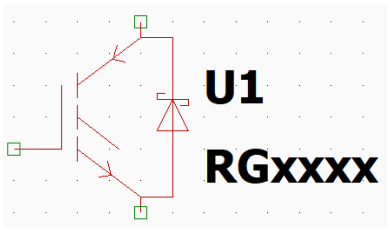
Symbol file name: IGBT-frd-therm.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 64 8 64 0
LINE Normal 64 8 64 8
LINE Normal 24 64 24 32
LINE Normal 0 64 24 64
LINE Normal 80 88 80 8
LINE Normal 64 8 80 8
LINE Normal 64 96 64 88
LINE Normal 64 88 80 88
LINE Normal 88 55 72 55
LINE Normal 80 39 88 55
LINE Normal 72 55 80 39
LINE Normal 88 39 72 39
LINE Normal 32 54 32 42
LINE Normal 32 38 32 26
LINE Normal 32 70 32 58
LINE Normal 64 8 32 32
LINE Normal 64 88 32 64
LINE Normal 53 64 32 48
LINE Normal 47 70 49 77
LINE Normal 43 78 49 77
LINE Normal 56 20 50 19
LINE Normal 52 12 50 19
RECTANGLE Normal 352 96 160 16
WINDOW 0 96 32 Left 2
WINDOW 3 96 0 Left 2
SYMATTR Value RGxxxx
SYMATTR Prefix X
SYMATTR Description ROHM IGBT
SYMATTR ModelFile xxxx.lib
PIN 64 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName G
PINATTR SpiceOrder 2
PIN 64 96 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
PIN 192 96 BOTTOM 8
PINATTR PinName Tjm
PINATTR SpiceOrder 4
PIN 256 96 BOTTOM 8
PINATTR PinName Tjd
PINATTR SpiceOrder 5
PIN 352 32 RIGHT 8
PINATTR PinName Tc
PINATTR SpiceOrder 6
PIN 320 96 BOTTOM 8
PINATTR PinName Ta
PINATTR SpiceOrder 7
---- End ----------------------------------
```

Appendix 9 : Circuit symbol file
“IGBT with built-in Schottky barrier diode”

Symbol:



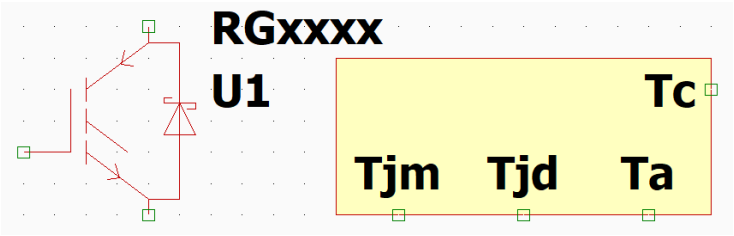
Symbol file name: IGBT-sbd.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 64 8 64 0
LINE Normal 64 8 64 8
LINE Normal 24 64 24 32
LINE Normal 0 64 24 64
LINE Normal 80 88 80 8
LINE Normal 64 8 80 8
LINE Normal 64 96 64 88
LINE Normal 64 88 80 88
LINE Normal 88 55 72 55
LINE Normal 80 39 88 55
LINE Normal 72 55 80 39
LINE Normal 88 39 72 39
LINE Normal 32 54 32 42
LINE Normal 32 38 32 26
LINE Normal 32 70 32 58
LINE Normal 64 8 32 32
LINE Normal 64 88 32 64
LINE Normal 53 64 32 48
LINE Normal 47 70 49 77
LINE Normal 43 78 49 77
LINE Normal 56 20 50 19
LINE Normal 52 12 50 19
LINE Normal 72 36 72 39
LINE Normal 76 36 72 36
LINE Normal 88 42 88 39
LINE Normal 84 42 88 42
WINDOW 0 96 32 Left 2
WINDOW 3 96 72 Left 2
SYMATTR Value RGxxxx
SYMATTR Prefix X
SYMATTR Description ROHM IGBT
SYMATTR ModelFile xxxx.lib
PIN 64 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName G
PINATTR SpiceOrder 2
PIN 64 96 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
---- End ------------------------------------
```

Appendix 10: Circuit symbol file
“IGBT with built-in Schottky barrier diode (coupled electro-thermal analysis model)”

Symbol:



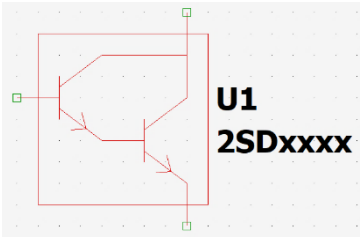
Symbol file name: IGBT-sbd-therm.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 64 8 64 0
LINE Normal 64 8 64 8
LINE Normal 24 64 24 32
LINE Normal 0 64 24 64
LINE Normal 80 88 80 8
LINE Normal 64 8 80 8
LINE Normal 64 96 64 88
LINE Normal 64 88 80 88
LINE Normal 88 55 72 55
LINE Normal 80 39 88 55
LINE Normal 72 55 80 39
LINE Normal 88 39 72 39
LINE Normal 32 54 32 42
LINE Normal 32 38 32 26
LINE Normal 32 70 32 58
LINE Normal 64 8 32 32
LINE Normal 64 88 32 64
LINE Normal 53 64 32 48
LINE Normal 47 70 49 77
LINE Normal 43 78 49 77
LINE Normal 56 20 50 19
LINE Normal 52 12 50 19
LINE Normal 72 36 72 39
LINE Normal 76 36 72 36
LINE Normal 88 42 88 39
LINE Normal 84 42 88 42
RECTANGLE Normal 352 96 160 16
WINDOW 0 96 32 Left 2
WINDOW 3 96 0 Left 2
SYMATTR Value RGxxxx
SYMATTR Prefix X
SYMATTR Description ROHM IGBT
SYMATTR ModelFile xxxx.lib
PIN 64 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName G
PINATTR SpiceOrder 2
PIN 64 96 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
PIN 192 96 BOTTOM 8
PINATTR PinName Tjm
PINATTR SpiceOrder 4
PIN 256 96 BOTTOM 8
PINATTR PinName Tjd
PINATTR SpiceOrder 5
PIN 352 32 RIGHT 8
PINATTR PinName Tc
PINATTR SpiceOrder 6
PIN 320 96 BOTTOM 8
PINATTR PinName Ta
PINATTR SpiceOrder 7
---- End ----------------------------------
```

Appendix 11: Circuit symbol file “Darlington Transistor NPN”

Symbol:



Symbol file name: Darlington-NPN1.asy

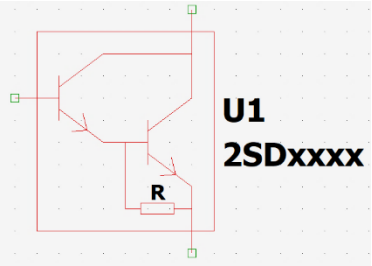
Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 96 112 96 80
LINE Normal 128 64 96 88
LINE Normal 128 128 96 104
LINE Normal 113 107 116 119
LINE Normal 105 120 116 119
LINE Normal 128 0 128 64
LINE Normal 128 160 128 128
LINE Normal 144 16 16 16
LINE Normal 144 144 144 16
LINE Normal 16 144 144 144
LINE Normal 16 16 16 144
LINE Normal 64 96 96 96
LINE Normal 32 72 64 96
LINE Normal 32 48 32 80
LINE Normal 0 64 32 64
LINE Normal 32 56 64 32
LINE Normal 128 32 64 32
LINE Normal 49 75 52 87
LINE Normal 41 88 52 87
WINDOW 0 150 64 Left 2
WINDOW 3 150 96 Left 2
SYMATTR Value 2SDxxxx
SYMATTR Prefix X
SYMATTR Description ROHM Darlington NPN BJT model
SYMATTR ModelFile xxxx.lib
PIN 128 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName B
PINATTR SpiceOrder 2
PIN 128 160 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3

---- End ----------------------------------
```

Appendix 12: Circuit symbol file
“Darlington Transistor NPN with built-in resistor”

Symbol:



Symbol file name: Darlington-NPN2.asy

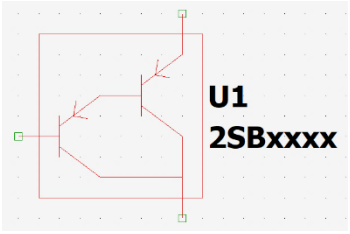
Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 96 112 96 80
LINE Normal 128 64 96 88
LINE Normal 128 128 96 104
LINE Normal 113 107 116 119
LINE Normal 105 120 116 119
LINE Normal 128 0 128 64
LINE Normal 128 176 128 128
LINE Normal 144 16 16 16
LINE Normal 144 160 144 16
LINE Normal 16 160 144 160
LINE Normal 16 16 16 160
LINE Normal 64 96 96 96
LINE Normal 32 72 64 96
LINE Normal 32 48 32 80
LINE Normal 0 64 32 64
LINE Normal 32 56 64 32
LINE Normal 128 32 64 32
LINE Normal 49 75 52 87
LINE Normal 41 88 52 87
LINE Normal 91 148 91 140
LINE Normal 115 148 91 148
LINE Normal 115 140 115 148
LINE Normal 91 140 115 140
LINE Normal 80 144 91 144
LINE Normal 80 96 80 144
LINE Normal 115 144 128 144
TEXT 98 132 Left 1 R
WINDOW 0 150 72 Left 2
WINDOW 3 150 104 Left 2
SYMATTR Value 2SDxxxx
SYMATTR Prefix X
SYMATTR Description ROHM Darlington NPN BJT model
SYMATTR ModelFile xxxx.lib
PIN 128 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName B
PINATTR SpiceOrder 2
PIN 128 176 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3

---- End ----------------------------------
```

Appendix 13: Circuit symbol file “Darlington Transistor PNP”

Symbol:



Symbol file name: Darlington-PNP1.asy

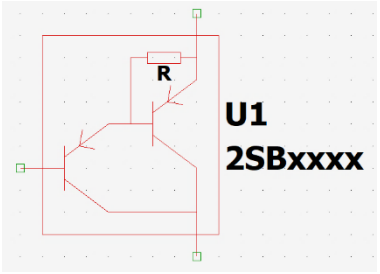
Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 96 80 96 48
LINE Normal 128 32 96 56
LINE Normal 128 96 96 72
LINE Normal 128 0 128 32
LINE Normal 128 160 128 96
LINE Normal 144 16 16 16
LINE Normal 144 144 144 16
LINE Normal 16 144 144 144
LINE Normal 16 16 16 144
LINE Normal 109 36 107 48
LINE Normal 118 50 107 48
LINE Normal 64 64 96 64
LINE Normal 32 88 64 64
LINE Normal 32 112 32 80
LINE Normal 32 96 0 96
LINE Normal 32 104 64 128
LINE Normal 128 128 64 128
LINE Normal 45 68 43 80
LINE Normal 54 82 43 80
WINDOW 0 148 64 Left 2
WINDOW 3 148 96 Left 2
SYMATTR Value 2SBxxxx
SYMATTR Prefix X
SYMATTR Description ROHM DIGITAL PNP BJT model
SYMATTR ModelFile xxxx.lib
PIN 128 160 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 96 NONE 0
PINATTR PinName B
PINATTR SpiceOrder 2
PIN 128 0 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3

---- End ----------------------------------
```

Appendix 14: Circuit symbol file
“Darlington Transistor PNP with built-in resistor”

Symbol:



Symbol file name: Darlington-PNP2.asy

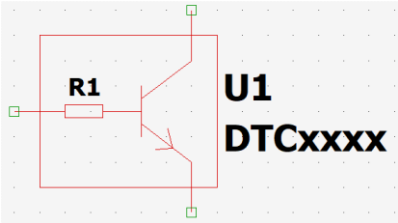
Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 96 96 96 64
LINE Normal 128 48 96 72
LINE Normal 128 112 96 88
LINE Normal 128 0 128 48
LINE Normal 128 176 128 112
LINE Normal 144 16 16 16
LINE Normal 144 160 144 16
LINE Normal 16 160 144 160
LINE Normal 16 16 16 160
LINE Normal 109 52 107 64
LINE Normal 118 66 107 64
LINE Normal 64 80 96 80
LINE Normal 32 104 64 80
LINE Normal 32 128 32 96
LINE Normal 32 112 0 112
LINE Normal 32 120 64 144
LINE Normal 128 144 64 144
LINE Normal 45 84 43 96
LINE Normal 54 98 43 96
LINE Normal 116 36 92 36
LINE Normal 116 28 116 36
LINE Normal 92 28 116 28
LINE Normal 92 36 92 28
LINE Normal 116 32 128 32
LINE Normal 80 32 92 32
LINE Normal 80 80 80 32
TEXT 99 43 Left 1 R
WINDOW 0 148 72 Left 2
WINDOW 3 148 104 Left 2
SYMATTR Value 2SBxxxx
SYMATTR Prefix X
SYMATTR Description ROHM DIGITAL PNP BJT model
SYMATTR ModelFile xxxx.lib
PIN 128 176 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 112 NONE 0
PINATTR PinName B
PINATTR SpiceOrder 2
PIN 128 0 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3

---- End ----------------------------------
```

Appendix 15: Circuit symbol file “Digital Transistor NPN with built-in R1”

Symbol:



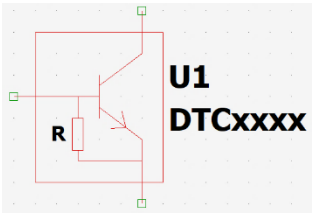
Symbol file name: DigitalTransistor-NPN1.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 80 80 80 48
LINE Normal 112 32 80 56
LINE Normal 112 96 80 72
LINE Normal 97 75 100 87
LINE Normal 89 88 100 87
LINE Normal 112 0 112 32
LINE Normal 56 60 32 60
LINE Normal 56 68 56 60
LINE Normal 32 68 56 68
LINE Normal 32 60 32 68
LINE Normal 0 64 32 64
LINE Normal 80 64 56 64
LINE Normal 112 128 112 96
LINE Normal 128 16 16 16
LINE Normal 128 112 128 16
LINE Normal 16 112 128 112
LINE Normal 16 16 16 112
TEXT 34 48 Left 1 R1
WINDOW 0 132 48 Left 2
WINDOW 3 132 80 Left 2
SYMATTR Value DTCxxxx
SYMATTR Prefix X
SYMATTR Description ROHM DIGITAL NPN BJT model
SYMATTR ModelFile xxxx.lib
PIN 112 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName B
PINATTR SpiceOrder 2
PIN 112 128 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
---- End ----------------------------------
```

Appendix 16: Circuit symbol file “Digital Transistor NPN with built-in R”

Symbol:



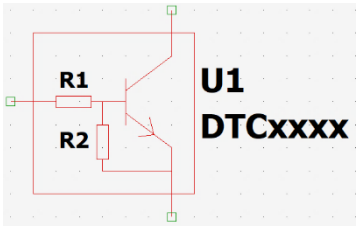
Symbol file name: DigitalTransistor-NPN2.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 64 80 64 48
LINE Normal 96 32 64 56
LINE Normal 96 96 64 72
LINE Normal 81 75 84 87
LINE Normal 73 88 84 87
LINE Normal 96 0 96 32
LINE Normal 44 104 44 80
LINE Normal 52 104 44 104
LINE Normal 52 80 52 104
LINE Normal 44 80 52 80
LINE Normal 96 112 48 112
LINE Normal 96 144 96 96
LINE Normal 112 16 16 16
LINE Normal 112 128 112 16
LINE Normal 16 128 112 128
LINE Normal 16 16 16 128
LINE Normal 48 80 48 64
LINE Normal 48 104 48 112
LINE Normal 64 64 0 64
TEXT 28 91 Left 1 R
WINDOW 0 116 48 Left 2
WINDOW 3 116 80 Left 2
SYMATTR Value DTCxxxx
SYMATTR Prefix X
SYMATTR Description ROHM DIGITAL NPN BJT model
SYMATTR ModelFile xxxx.lib
PIN 96 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName B
PINATTR SpiceOrder 2
PIN 96 144 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
---- End ----------------------------------
```

Appendix 17: Circuit symbol file
“Digital Transistor NPN with built-in R1 and R2”

Symbol:



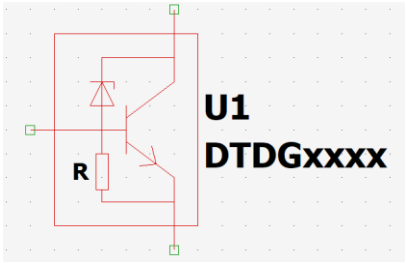
Symbol file name: .asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 80 80 80 48
LINE Normal 112 32 80 56
LINE Normal 112 96 80 72
LINE Normal 97 75 100 87
LINE Normal 89 88 100 87
LINE Normal 112 0 112 32
LINE Normal 56 60 32 60
LINE Normal 56 68 56 60
LINE Normal 32 68 56 68
LINE Normal 32 60 32 68
LINE Normal 60 104 60 80
LINE Normal 68 104 60 104
LINE Normal 68 80 68 104
LINE Normal 60 80 68 80
LINE Normal 0 64 32 64
LINE Normal 80 64 56 64
LINE Normal 112 112 64 112
LINE Normal 112 144 112 96
LINE Normal 128 16 16 16
LINE Normal 128 128 128 16
LINE Normal 16 128 128 128
LINE Normal 16 16 16 128
LINE Normal 64 80 64 64
LINE Normal 64 104 64 112
TEXT 34 48 Left 1 R1
TEXT 34 90 Left 1 R2
WINDOW 0 132 48 Left 2
WINDOW 3 132 80 Left 2
SYMATTR Value DTCxxxx
SYMATTR Prefix X
SYMATTR Description ROHM DIGITAL NPN BJT model
SYMATTR ModelFile xxxx.lib
PIN 112 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName B
PINATTR SpiceOrder 2
PIN 112 144 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
---- End ------------------------------------
```

Appendix 18: Circuit symbol file
“Digital Transistor NPN with built-in R and Zener diode”

Symbol:



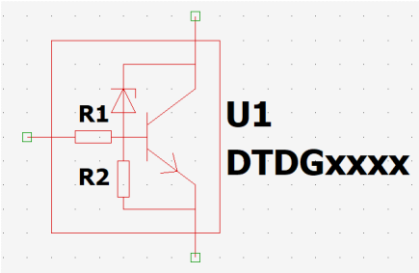
Symbol file name: DigitalTransistor-NPN4.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 64 96 64 64
LINE Normal 96 48 64 72
LINE Normal 96 112 64 88
LINE Normal 81 91 84 103
LINE Normal 73 104 84 103
LINE Normal 96 0 96 48
LINE Normal 44 120 44 96
LINE Normal 52 120 44 120
LINE Normal 52 96 52 120
LINE Normal 44 96 52 96
LINE Normal 96 128 48 128
LINE Normal 96 160 96 112
LINE Normal 112 16 16 16
LINE Normal 112 144 112 16
LINE Normal 16 144 112 144
LINE Normal 16 16 16 144
LINE Normal 48 120 48 128
LINE Normal 56 48 40 48
LINE Normal 56 64 40 64
LINE Normal 48 48 56 64
LINE Normal 40 64 48 48
LINE Normal 56 53 56 48
LINE Normal 0 80 64 80
LINE Normal 48 32 96 32
LINE Normal 48 96 48 32
TEXT 28 107 Left 1 R
WINDOW 0 116 64 Left 2
WINDOW 3 116 96 Left 2
SYMATTR Value DTDGxxxx
SYMATTR Prefix X
SYMATTR Description ROHM DIGITAL NPN BJT model
SYMATTR ModelFile xxxx.lib
PIN 96 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 80 NONE 0
PINATTR PinName B
PINATTR SpiceOrder 2
PIN 96 160 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
---- End ----------------------------------
```

Appendix 19: Circuit symbol file
“Digital Transistor NPN with built-in R1 R2 and Zener diode”

Symbol:



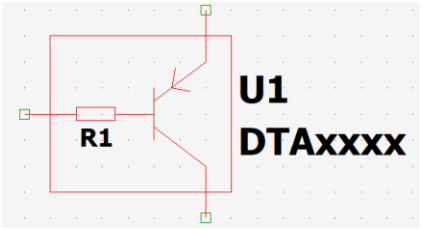
Symbol file name: .asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 80 96 80 64
LINE Normal 112 48 80 72
LINE Normal 112 112 80 88
LINE Normal 97 91 100 103
LINE Normal 89 104 100 103
LINE Normal 112 0 112 48
LINE Normal 56 76 32 76
LINE Normal 56 84 56 76
LINE Normal 32 84 56 84
LINE Normal 32 76 32 84
LINE Normal 60 120 60 96
LINE Normal 68 120 60 120
LINE Normal 68 96 68 120
LINE Normal 60 96 68 96
LINE Normal 0 80 32 80
LINE Normal 80 80 56 80
LINE Normal 112 128 64 128
LINE Normal 112 160 112 112
LINE Normal 128 16 16 16
LINE Normal 128 144 128 16
LINE Normal 16 144 128 144
LINE Normal 16 16 16 144
LINE Normal 64 120 64 128
LINE Normal 72 48 56 48
LINE Normal 72 54 72 48
LINE Normal 72 64 56 64
LINE Normal 64 48 72 64
LINE Normal 56 64 64 48
LINE Normal 64 32 112 32
LINE Normal 64 96 64 32
TEXT 34 64 Left 1 R1
TEXT 34 106 Left 1 R2
WINDOW 0 132 64 Left 2
WINDOW 3 132 96 Left 2
SYMATTR Value DTDGxxxx
SYMATTR Prefix X
SYMATTR Description ROHM DIGITAL NPN BJT model
SYMATTR ModelFile xxxx.lib
PIN 112 0 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 80 NONE 0
PINATTR PinName B
PINATTR SpiceOrder 2
PIN 112 160 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
---- End ----------------------------------
```

Appendix 20: Circuit symbol file “Digital Transistor PNP with built-in R1”

Symbol:



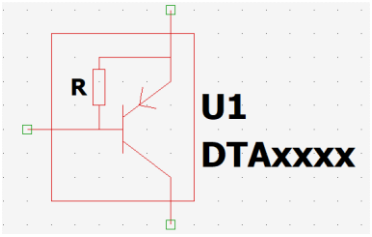
Symbol file name: DigitalTransistor-PNP1.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 80 80 80 48
LINE Normal 112 32 80 56
LINE Normal 112 96 80 72
LINE Normal 112 0 112 32
LINE Normal 56 60 32 60
LINE Normal 56 68 56 60
LINE Normal 32 68 56 68
LINE Normal 32 60 32 68
LINE Normal 0 64 32 64
LINE Normal 80 64 56 64
LINE Normal 112 128 112 96
LINE Normal 128 16 16 16
LINE Normal 128 112 128 16
LINE Normal 16 112 128 112
LINE Normal 16 16 16 112
LINE Normal 93 36 91 48
LINE Normal 102 50 91 48
TEXT 34 78 Left 1 R1
WINDOW 0 132 48 Left 2
WINDOW 3 132 80 Left 2
SYMATTR Value DTAxxxx
SYMATTR Prefix X
SYMATTR Description ROHM DIGITAL PNP BJT model
SYMATTR ModelFile xxxx.lib
PIN 112 128 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 64 NONE 0
PINATTR PinName B
PINATTR SpiceOrder 2
PIN 112 0 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
---- End ----------------------------------
```

Appendix 21: Circuit symbol file “Digital Transistor PNP with built-in R”

Symbol:



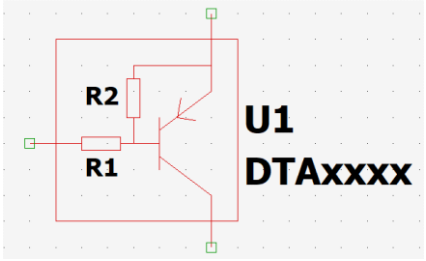
Symbol file name: DigitalTransistor-PNP2.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 64 96 64 64
LINE Normal 96 48 64 72
LINE Normal 96 112 64 88
LINE Normal 96 0 96 48
LINE Normal 44 64 44 40
LINE Normal 52 64 44 64
LINE Normal 52 40 52 64
LINE Normal 44 40 52 40
LINE Normal 96 32 48 32
LINE Normal 96 144 96 112
LINE Normal 112 16 16 16
LINE Normal 112 128 112 16
LINE Normal 16 128 112 128
LINE Normal 16 16 16 128
LINE Normal 48 80 48 64
LINE Normal 48 32 48 40
LINE Normal 77 52 75 64
LINE Normal 86 66 75 64
LINE Normal 64 80 0 80
TEXT 29 51 Left 1 R
WINDOW 0 116 64 Left 2
WINDOW 3 116 96 Left 2
SYMATTR Value DTAxxxx
SYMATTR Prefix X
SYMATTR Description ROHM DIGITAL PNP BJT model
SYMATTR ModelFile xxxx.lib
PIN 96 144 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 80 NONE 0
PINATTR PinName B
PINATTR SpiceOrder 2
PIN 96 0 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
---- End ----------------------------------
```

Appendix 22: Circuit symbol file
“Digital Transistor PNP with built-in R1 and R2”

Symbol:



Symbol file name: DigitalTransistor-PNP3.asy

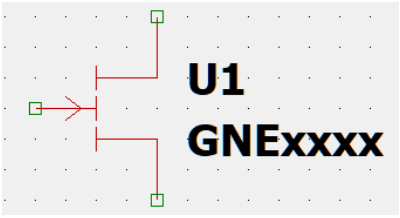
Text data:

```
---- Start ----------------------------------
Version 4
SymbolType CELL
LINE Normal 80 96 80 64
LINE Normal 112 48 80 72
LINE Normal 112 112 80 88
LINE Normal 112 0 112 48
LINE Normal 56 76 32 76
LINE Normal 56 84 56 76
LINE Normal 32 84 56 84
LINE Normal 32 76 32 84
LINE Normal 60 64 60 40
LINE Normal 68 64 60 64
LINE Normal 68 40 68 64
LINE Normal 60 40 68 40
LINE Normal 0 80 32 80
LINE Normal 80 80 56 80
LINE Normal 112 32 64 32
LINE Normal 112 144 112 112
LINE Normal 128 16 16 16
LINE Normal 128 128 128 16
LINE Normal 16 128 128 128
LINE Normal 16 16 16 128
LINE Normal 64 80 64 64
LINE Normal 64 32 64 40
LINE Normal 93 52 91 64
LINE Normal 102 66 91 64
TEXT 34 94 Left 1 R1
TEXT 34 50 Left 1 R2
WINDOW 0 132 64 Left 2
WINDOW 3 132 96 Left 2
SYMATTR Value DTAxxxx
SYMATTR Prefix X
SYMATTR Description ROHM DIGITAL PNP BJT model
SYMATTR ModelFile xxxx.lib
PIN 112 144 NONE 0
PINATTR PinName C
PINATTR SpiceOrder 1
PIN 0 80 NONE 0
PINATTR PinName B
PINATTR SpiceOrder 2
PIN 112 0 NONE 0
PINATTR PinName E
PINATTR SpiceOrder 3
---- End ----------------------------------
```

Appendix 23: Circuit symbol file

“GaN HEMT 3-pin”

Symbol:



Symbol file name: GaNhemt-3.asy

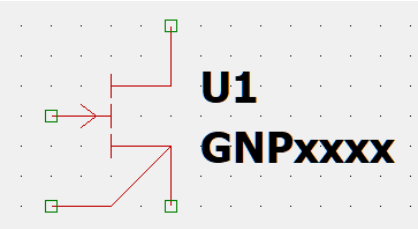
Text data:

```
---- Start ----------------------------------
Version 4
SymbolType BLOCK
LINE Normal 32 38 32 26
LINE Normal 32 54 32 42
LINE Normal 32 70 32 58
LINE Normal 64 32 32 32
LINE Normal 64 64 32 64
LINE Normal 64 32 64 0
LINE Normal 64 64 64 96
LINE Normal 32 48 0 48
LINE Normal 24 48 16 42
LINE Normal 16 54 24 48
WINDOW 3 80 64 Left 2
WINDOW 0 80 32 Left 2
SYMATTR Value GNExxxx
SYMATTR Prefix X
SYMATTR Description ROHM GaN HEMT
SYMATTR ModelFile xxxx.lib
PIN 64 0 NONE 8
PINATTR PinName D
PINATTR SpiceOrder 1
PIN 0 48 NONE 8
PINATTR PinName G
PINATTR SpiceOrder 2
PIN 64 96 NONE 8
PINATTR PinName S
PINATTR SpiceOrder 3
---- End ----------------------------------
```

Appendix 24: Circuit symbol file

“GaN HEMT 4-pin”

Symbol:



Symbol file name: GaNhemt-4.asy

Text data:

```
---- Start ----------------------------------
Version 4
SymbolType BLOCK
LINE Normal 32 38 32 26
LINE Normal 32 54 32 42
LINE Normal 32 70 32 58
LINE Normal 64 32 32 32
LINE Normal 64 64 32 64
LINE Normal 64 32 64 0
LINE Normal 64 64 64 96
LINE Normal 32 48 0 48
LINE Normal 32 96 64 64
LINE Normal 32 96 0 96
LINE Normal 24 48 16 42
LINE Normal 16 54 24 48
WINDOW 3 80 64 Left 2
WINDOW 0 80 32 Left 2
SYMATTR Value GNPxxxx
SYMATTR Prefix X
SYMATTR Description ROHM GaN HEMT
SYMATTR ModelFile xxxx.lib
PIN 64 0 NONE 8
PINATTR PinName D
PINATTR SpiceOrder 1
PIN 0 48 NONE 8
PINATTR PinName G
PINATTR SpiceOrder 2
PIN 0 96 NONE 8
PINATTR PinName KS
PINATTR SpiceOrder 3
PIN 64 96 NONE 8
PINATTR PinName S
PINATTR SpiceOrder 4
---- End ----------------------------------
```

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